2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA

accellera SYSTEMS INITIATIVE

Avery Verification IP: Delivering Accelerated Confidence in Complex IC Verification

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SIEMENS

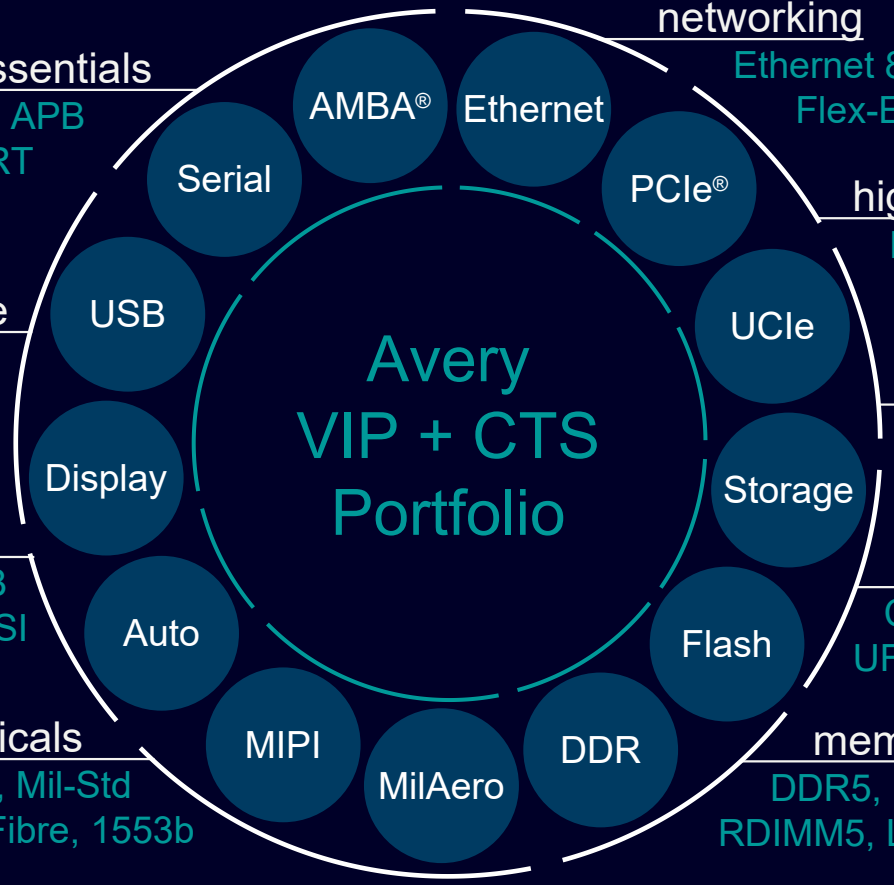
Avery Verification IP – Delivering Accelerated Confidence

Accelerated

- First To Market AND high quality via partnerships
- Fast standard SV/UVM runs on all engines
- Sim Acceleration on emulator and prototype system
- Supports QEMU co-simulation for HW/SW co-dev

Confidence

- Tested on multiple controller designs from IP Partners
- CTS Finds bugs in design IPs that other VIPs miss
- Future-proof Roadmap and Packaging
- Broad Portfolio: Verification IPs + Compliance Tests



SoC essentials
CHI, ACE5, AXI5, AHB, APB
CXS, TileLink, JTAG, UART
SMBus, SPI/xSPI, I2C/I3C/I2S

human interface
USB4, USB3.2, PD, SoundWire
HDMI2.1a, DP2.0, DPI, SFPDP

automotive net
10M-10G T1 Auto Ethernet, TSN/AVB
CAN/LIN, Flexray, MIPI CSI/DSI

mil-aero verticals
PCI, JESD204, SRIO, Mil-Std
SpaceWire, SpaceFibre, 1553b

networking
Ethernet 800G/1600G, MacSec
Flex-E, BaseT, UEC, UALink, Infiniband

high-perf compute
PCIe5/6/Gen7 interconnect
CCIX, CXL 2.0/3.0/3.1/3.2

3DIC/chiplet
UCIe 1.1/2.0, BoW, C2C, HBM2E/3/4
Custom Solutions & Services

high-perf storage
CXL2/3, NVMe, UAS, SAS, SATA, AHCI,
UFS4, eMMC, SD, ONFI, Flash/SSD stds

memory models
DDR5, LPDDR5/6, GDDR6/7, DFI
RDIMM5, LRDIMM5, MRDIMM5, HBM4

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Future-proof Roadmap and Packaging

Broad Portfolio: Verification IPs + Compliance Tests

Accelerate your Time To Market:

Early adoption mentality:

- we invest to be **first to market** with usable VIP (e.g. PCIe7, CXL3.2, UCIe2.0, UALink)

- we work with **bleeding edge** partners on **new/emerging protocols**
  E.g. Intel, Astera, Comira, Rambus, Alphawave

This success **builds confidence and trust** in turn:

- E.g. we are the main developer of Compliance Tests used by the CXL consortium
- Our technical lead delivers seamless integration, deeper coverage, higher quality
- Even customers who use other VIPs in testbenches, use Avery VIP for signoff

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Accelerate your Time To Market **in 3DIC**:

UCIe™ Universal Chiplet Interconnect Express

2.0 available now

View our technical webinar from Aug 21st on Verification Academy

Our statement of support in the UCIe2.0 launch on Aug 6 2024:

"Building on our leadership in chiplets technology and strong track record of support for the standard, Siemens EDA is once again a key contributor for the newest version of UCIe technology. With our UCIe2.0 Verification IP and Compliance Test Suite solutions, Siemens continues its UCIe design verification leadership. And because version 2.0 of the UCIe standard incorporates advances that support mainstream design for test (DFT) practices, it paves the way for next-generation products capable of fully leveraging Siemens' industry-leading Tessent software."

Mike Ellow, CEO of Silicon Systems for Siemens EDA

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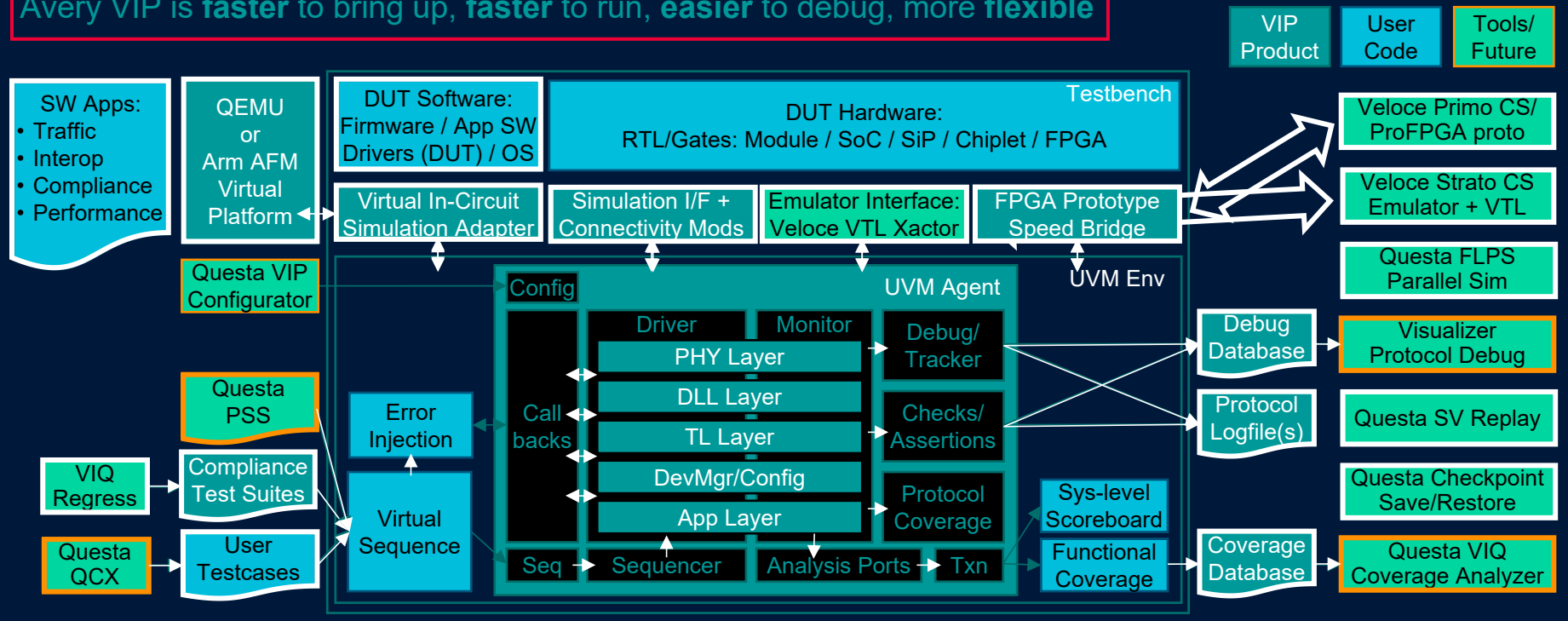
Future-proof Roadmap and Packaging

Broad Portfolio: Verification IPs + Compliance Tests

- SV/UVM Compliant
  - Extensible APIs
- VIP Configurator
  - Creates full TB
- VIQ Integration
  - Coverage mgmt
- VIZ Integration
  - Easy debug
- Simulator Agnostic
  - Questa Optimized
- Simulation acceleration
  - VIP+VTL solutions
- FPGA prototype IP
  - Speed Adapters
- HW/SW Cosim
  - Virtual / QEMU

Customer feedback: Other VIPs are slower and less capable:
Avery VIP is **faster** to bring up, **faster** to run, **easier** to debug, more **flexible**



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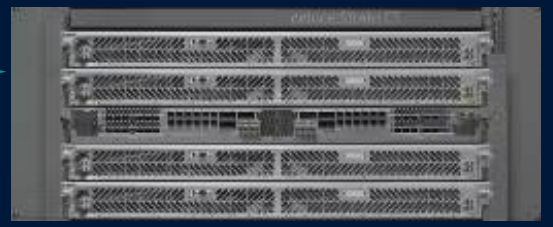
Accelerating Simulation VIP based Testbenches using Veloce Emulation Hardware

Customers: “how can I get the most from my Veloce CS emulator investment? I want to keep all my existing simulation testbench and stimulus, and **accelerate**...”



RTL Design + UVM Sim TB → Port RTL DESIGN to Veloce → Fast Forward with **Accelerated** VIP Solution – reuse testbench and stimulus
Accelerated VIP supports Questa, Veloce, Primo → **Accelerated** Design+TB

- **Simulation Acceleration:**
  - Avery VIP running in conjunction with Veloce VTL on Veloce Strato CS emulation, Veloce Primo CS prototyping
- Provides 50-90x speed up vs pure simulation:
  - Enables reuse of testbench and VIP test cases / UVM sequences between engines

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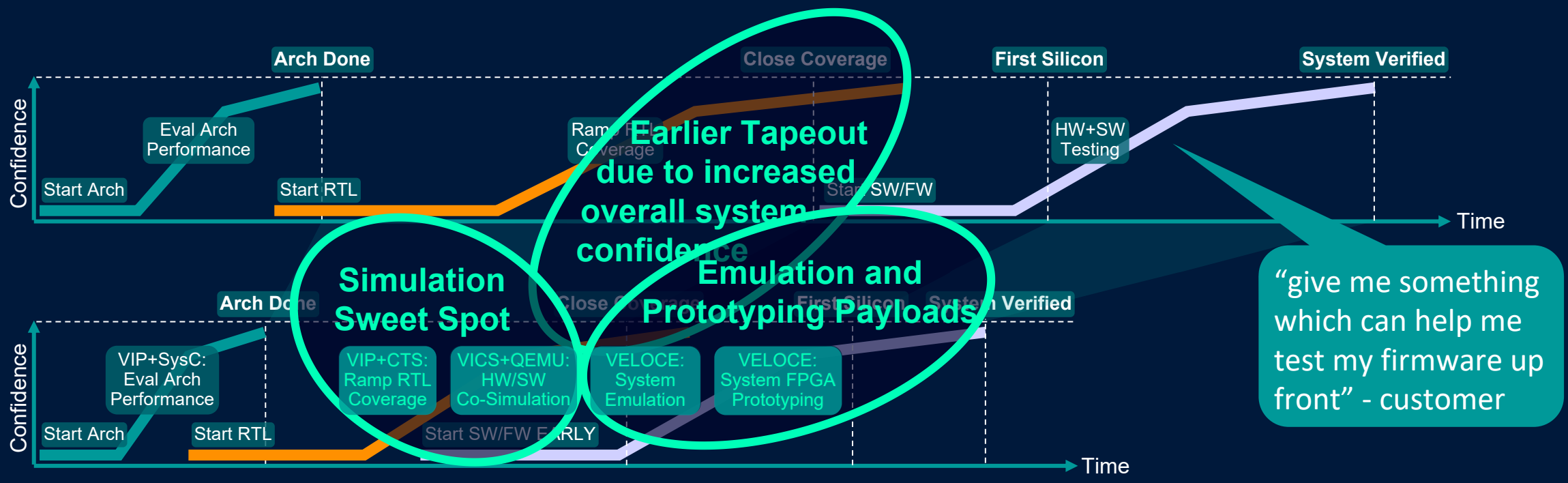
Questa Software-Aware VIP - a seamless shift **from Sequences to Software**, accelerating HW/SW signoff



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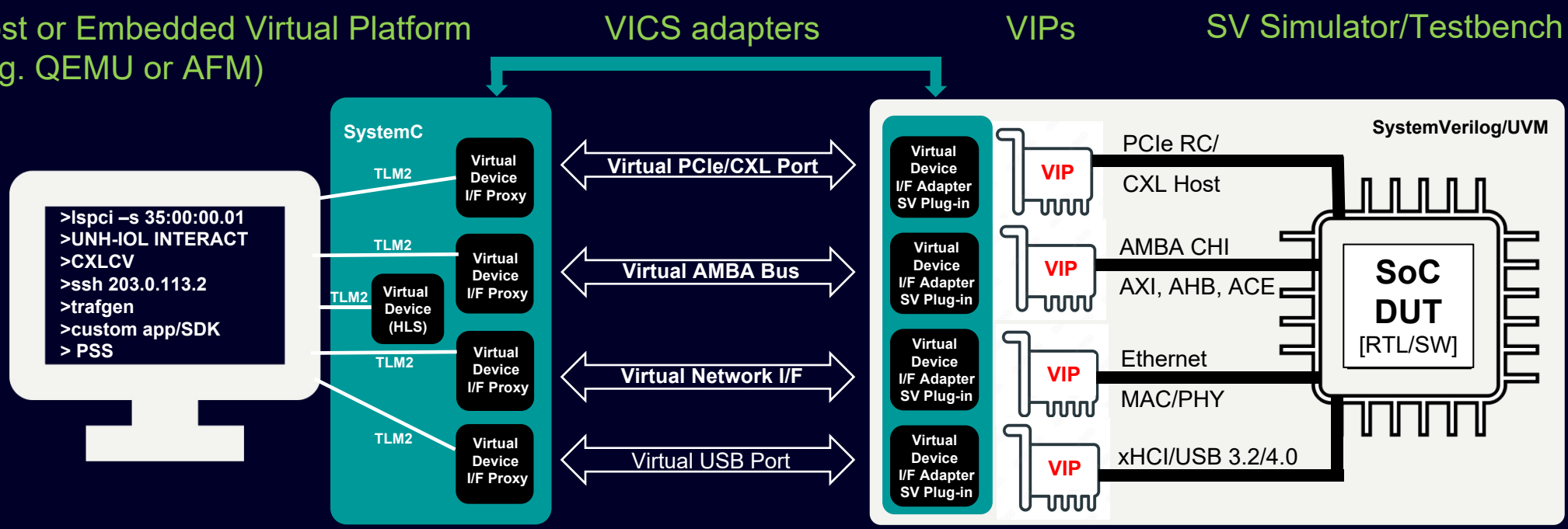
Virtual In-Circuit Simulation – a seamless shift **from Sequences to Software**, accelerating HW/SW signoff



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Delivering **Confidence** via partner design testing:

- **Multiple IP partnerships** for mutual validation and reach
- We use multiple controllers and multiple designs to **test our VIP**
- Ensure our solutions are **Seamless** and **Easy to Deploy**

ALPHAWAVE SEMI	ANALOG BITS	arasan Total IP	CAST Silicon IP Cores	
PCIe CXL UCIe Ethernet	PCIe PHY	I3C CSI DSI UFS Uunipro Ethernet CAN	CAN Ethernet LIN	UCIe CUSTOM
CoMIRA SOLUTIONS	Corigine	etopus we accelerate	mobiveil Investors in Innovation	
PCIe CXL UCIe Ethernet	USB xHCI	PCIe/CXL/UCIe	NVMe ONFI DDR5	
Rambus	Silicon Library	SignatureIP	iol University of New Hampshire InterOperability Laboratory	AMD XILINX
PCIe CXL HBM GDDR LPDDR GDDR	DisplayPort	PCIe	Ethernet	PCIe

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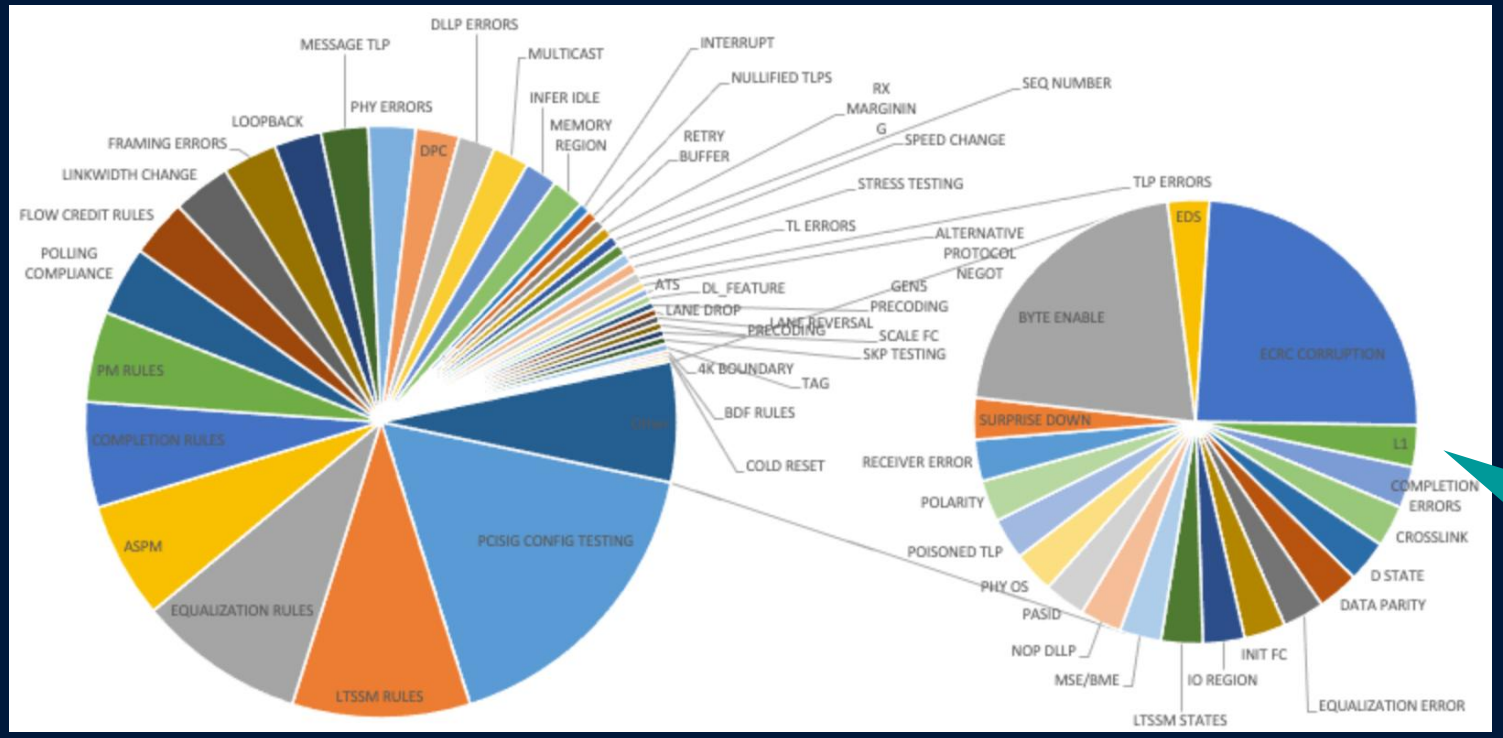
Build vs Buy? Rely on Avery VIP+CTS for compliance/quality, freeing up your resources



- **Avery Compliance Test Suites:**
- Covers whole spec, not just std tests
- Constrained-random SV/UVM code
- Full test plan and coverage model
- Still finding PCIe5 bugs in IP configs
- **Industry's signoff VIP / test suite**

"you found an IP bug the IP vendor VIP did not catch – with just ONE test"
– HPC customer

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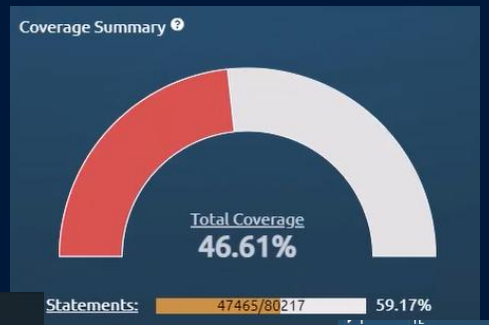
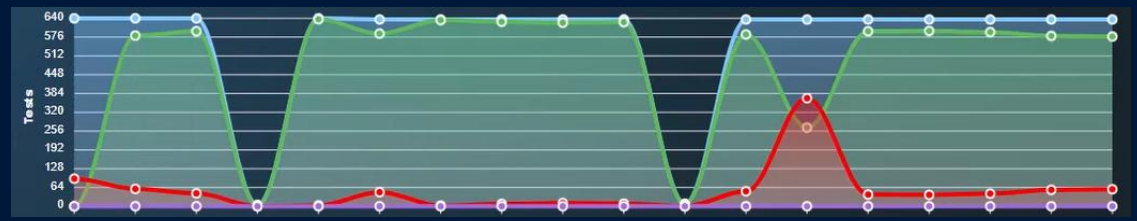
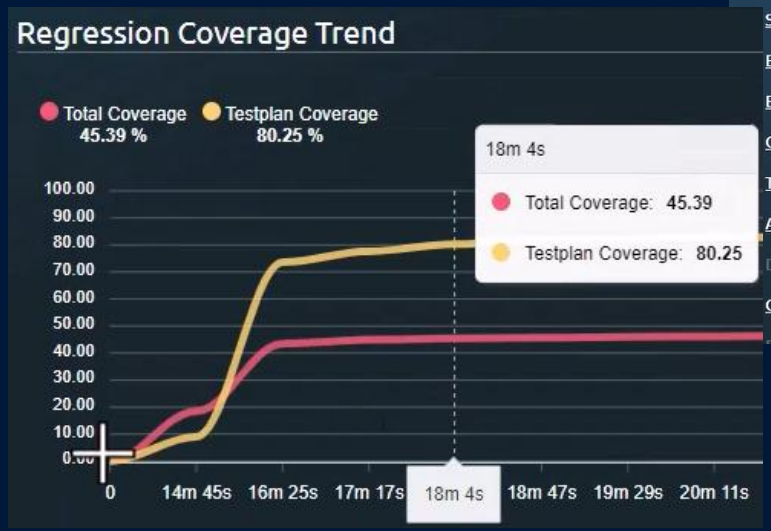
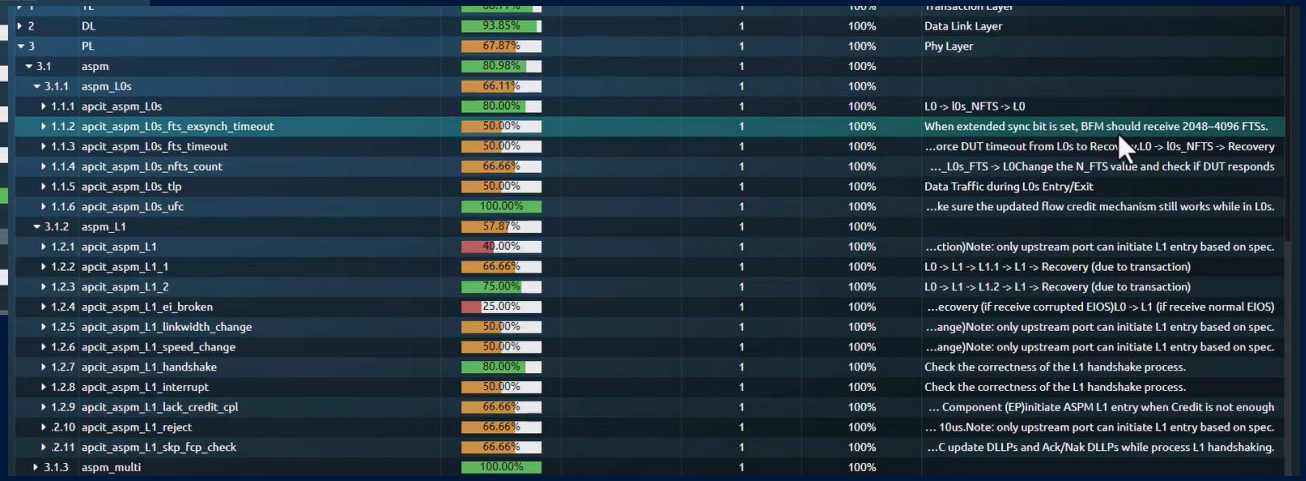
Seamless flow for managing complex protocol Test Suites and closing Coverage









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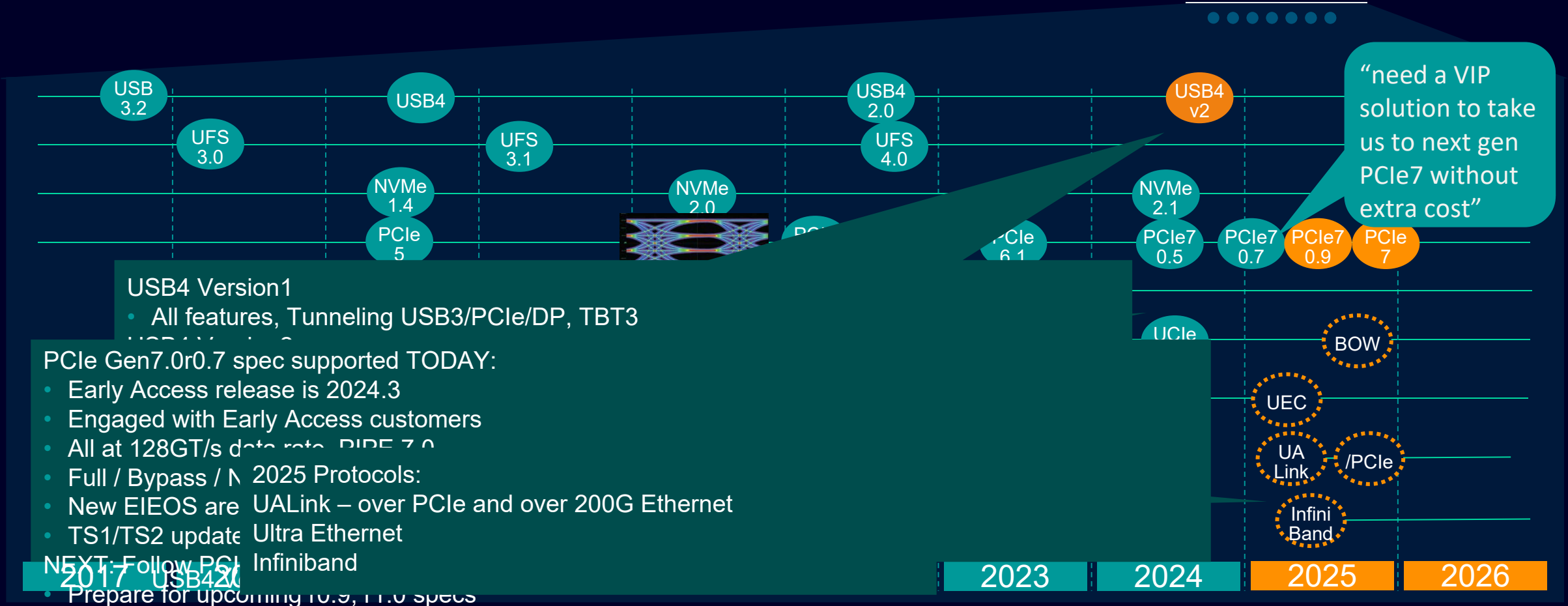

USB4 Version1
- All features, Tunneling USB3/PCIe/DP, TBT3

PCIe Gen7.0r0.7 spec supported TODAY:
- Early Access release is 2024.3
- Engaged with Early Access customers
- All at 128GT/s data rate, PIPE 7.0
- Full / Bypass / N
- New EIEOS are
- TS1/TS2 update

NEXT: Follow PCI
- Prepare for upcoming r0.9, r1.0 specs
  - Typically, VIP available 2 weeks after spec
  - Broader customer release at spec r0.9

2025 Protocols:
- UALink – over PCIe and over 200G Ethernet
- Ultra Ethernet
- Infiniband

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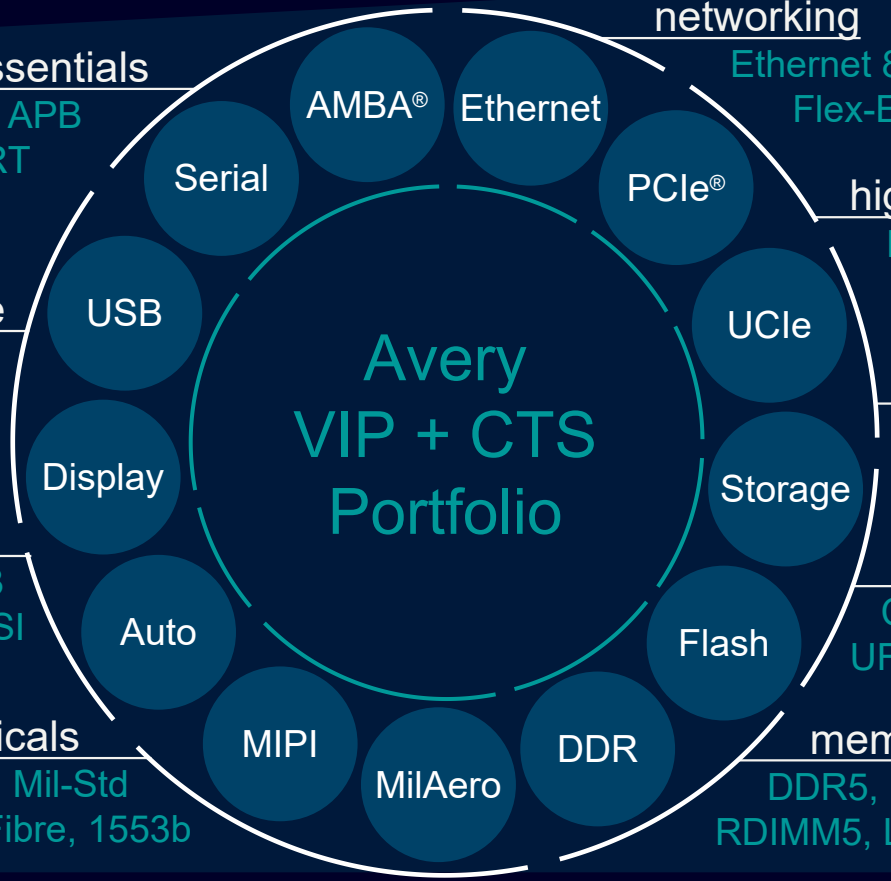

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CHI, ACE5, AXI5, AHB, APB
CXS, TileLink, JTAG, UART
SMBus, SPI/xSPI, I2C/I3C/I2S

human interface
USB4, USB3.2, PD, SoundWire
HDMI2.1a, DP2.0, DPI, SFPDP

automotive net
10M-10G T1 Auto Ethernet, TSN/AVB
CAN/LIN, Flexray, MIPI CSI/DSI

mil-aero verticals
PCI, JESD204, SRIO, Mil-Std
SpaceWire, SpaceFibre, 1553b

networking
Ethernet 800G/1600G, MacSec
Flex-E, BaseT, UEC, UALink, Infiniband

high-perf compute
PCIe5/6/Gen7 interconnect
CCIX, CXL 2.0/3.0/3.1/3.2

3DIC/chiplet
UCIe 1.1/2.0, BoW, C2C, HBM2E/3/4
Custom Solutions & Services

high-perf storage
CXL2/3, NVMe, UAS, SAS, SATA, AHCI,
UFS4, eMMC, SD, ONFI, Flash/SSD stds

memory models
DDR5, LPDDR5/6, GDDR6/7, DFI
RDIMM5, LRDIMM5, MRDIMM5, HBM4

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Thank You!

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