2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA

accellera SYSTEMS INITIATIVE

Multi-cycle path verification method based on TCM

Qiudong Xiang, KUNLUNXIN (Beijing) Technology Co., Ltd.
Wenping Guo, KUNLUNXIN (Beijing) Technology Co., Ltd.
Donghui Xie, Synopsys Technology (Beijing) Co., Ltd.

16 Apr 2025 上海 SHANGHAI

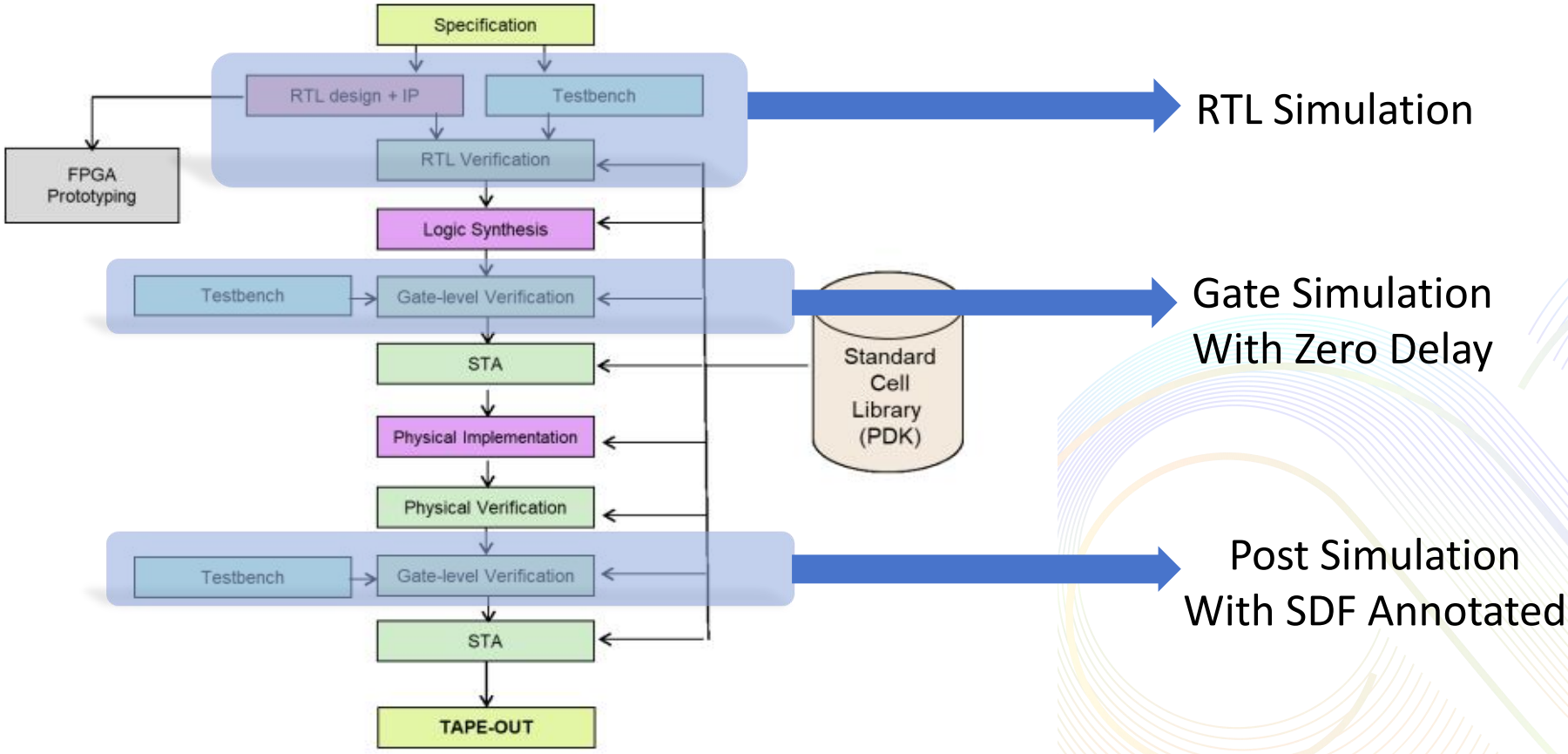
KUNLUNXIN

Agenda

- Introduction
  - Existing SDC Verification Challenges
  - Synopsys SDC Solutions
- TCM Verification
  - The Flow of Formal Verification of MCP Using TCM
  - The Environmental Framework for TCM verification
  - The results of TCM verification
- Dynamic Verification
  - VCS With SDC/SVA Simulation Flow
  - VCS SDC RTL Simulation Result
- CONCLUSION & FUTURE WORK

Existing SDC Verification Challenges

3-Stage of Verification Flow: RTL/Gate/Post-Sim



RTL-Sim focus on RTL functional issues, Only Post-Sim carry the exact timing delay information

Existing SDC Verification Challenges

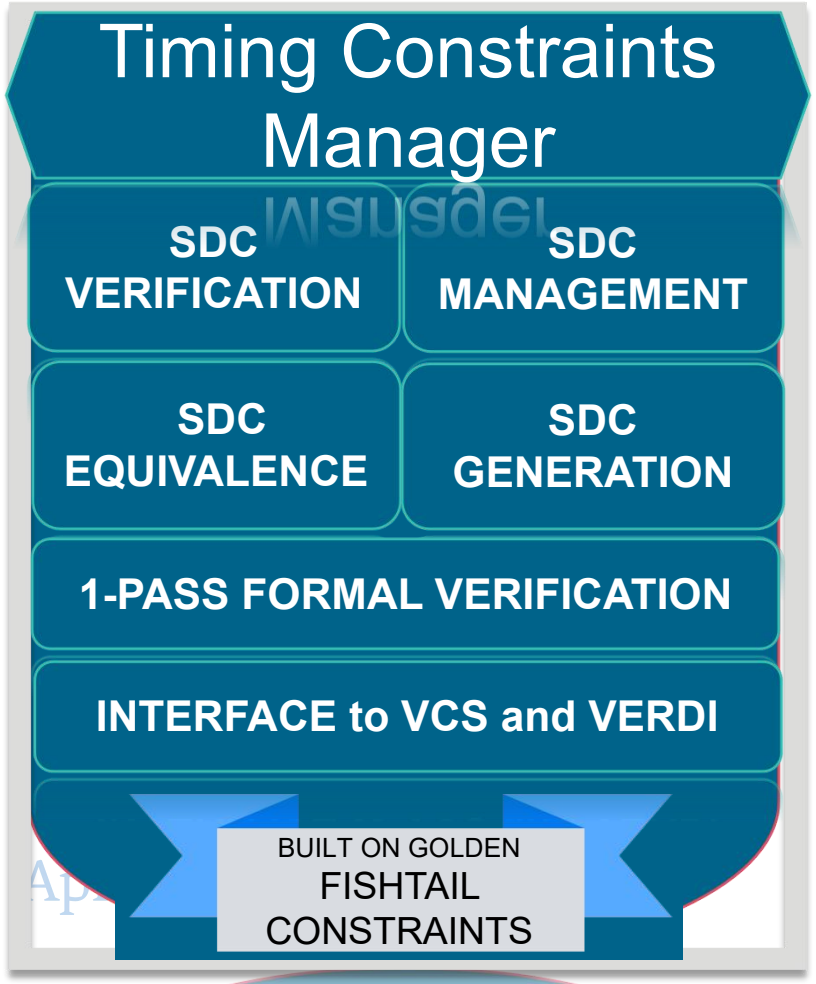
Performance Comparison of RTL/Gate/Post-Sim

CASE	COMMAND	RTL SIM	GATE SIM	POST SIM
Same Test	simv	1.9h	23.5h	460h = ~19day
	elab	1.5h	4.2h	24.7h
	analysis	11min	90s(copy)	113s(copy)
	memory	13G	306G	682G POSTSIM/RTLSIM=52

Traditional SDC Verification covered by POST SIM, Too much TAT and Late for fixing Found MCP/FP Bugs!!!

Synopsys Timing Constraints Manager

Built on FishTail Best-in-Class SDC Constraints Solution



- Comprehensive SDC Timing Constraints Generation, Verification and Management
- Multi-Cycle/False Path Exception Verification with No Noise
  RTL Designers are provided precise feedback on their SDC bugs
- Comprehensive SDC Management solution
  Tape-out proven promotion, demotion, mapping solution
- Automated SDC Generation from RTL
  Saves weeks of designer effort and development schedule

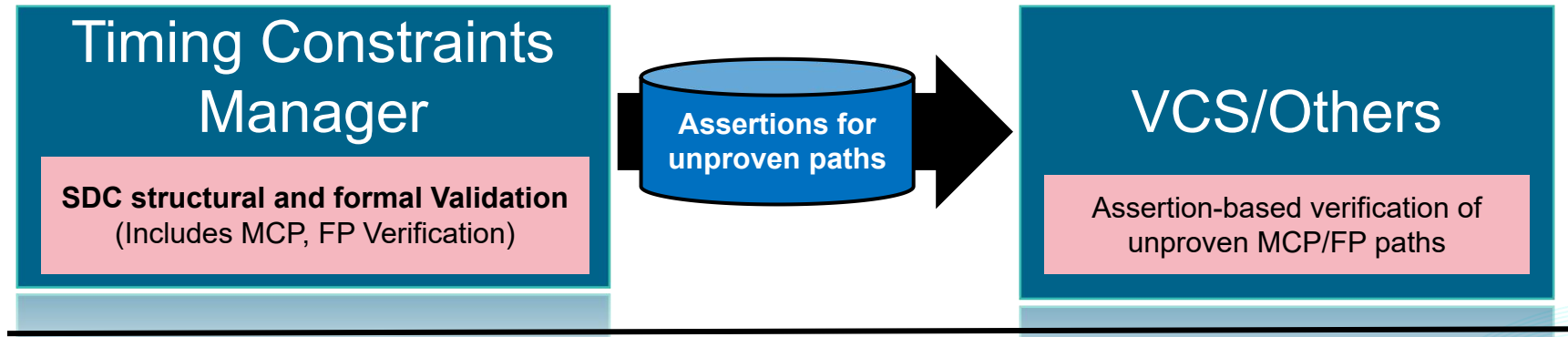
90% Reduction in Designer SDC Review Effort

Auto SDC Gen/Mgmt shortens SoC Execution by **6-8 Weeks**

Eliminate silicon failure from SDC bugs

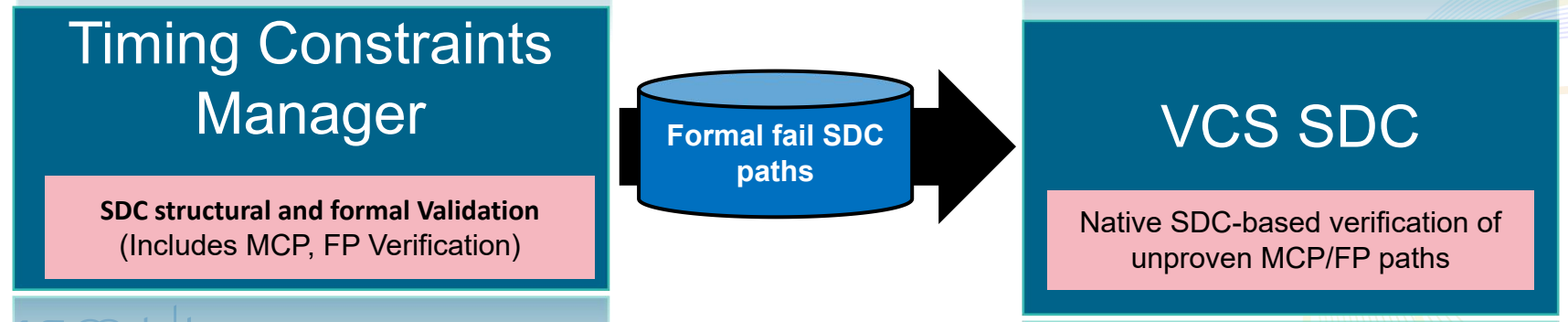
Verify MCP/FP with Both TCM Formal engine and VCS/SDC

SDC Verification Using TCM involves multiple flows



Flow 1: TCM to VCS/3rd party simulators

- Assertion based
- Applicable for HardMacro
- Support VHDL



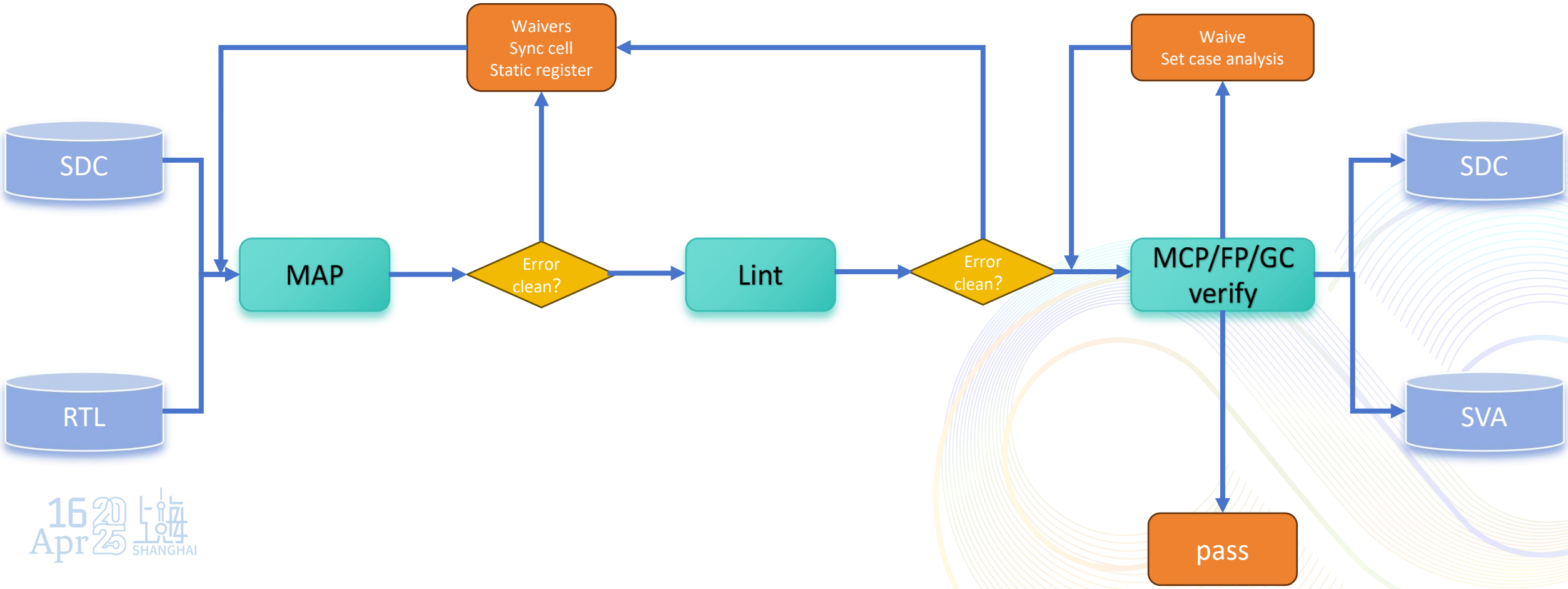
Flow 2: TCM to VCS SDC

- Native SDC-based
- Easy to debug
- MCP/FP coverage tracking

User Can adopt either TCM SVA Flow or TCM + VCS SDC Flow based on Design Statistics

TCM Verification

The Flow of Formal Verification of MCP Using TCM



TCM MAP

- Review TCM mapped SDC:
  - cd fishtail_rtl_verification/setup
  - gvim **top.syn.mapped.sdc**
- Friendly for Human Reading
  - Unroll the collection
  - Unroll the wildcard Object
  - Unroll the 'foreach'
  - Support tcl-based command

```
72 set rst_reg_ck [get_pins -of [get_cells -q -hier "rst_n_local_r_reg"] -filter full_name=~"*/CK"||full_name=~"*/clocked_on"]
73 if {[sizeof $rst_reg_ck]} {
74     set_multicycle_path -start -setup  7 -from $rst_reg_ck
75     set_multicycle_path -start -hold  13 -from $rst_reg_ck
76 }
```

```
680 set_multicycle_path \
681   -from { clkrst_apb_inst/rst_n_local_r_reg/clocked_on clkrst_cluster_ao_rst_inst/rst_n_local_r_reg/clocked_on \
682           clkrst_cluster_inst/rst_n_local_r_reg/clocked_on clkrst_core_inst/rst_n_local_r_reg/clocked_on } \
683   -setup \
684    7 \
685   -start
```

```
77 set_multicycle_path 3 -setup  -from apb_cfg_inst/wr_reg_pe_ena* -to clint_inst/clint*
78 set_false_path -from  apb_cfg_inst/wr_reg_pe_ena* -to clint_inst/clint*
```

```
632 set_multicycle_path \
633   -from { apb_cfg_inst/wr_reg_pe_ena_reg[*] } \
634   -to { clint_inst/clint0_reg clint_inst/clint1_reg clint_inst/clint2_reg clint_inst/clint_apb_rd_data_reg[*] clint_inst/clint_apb_rd_vld_reg } \
635   -setup \
636    3
637
```

```
foreach_in clka [all_clocks] {
    foreach_in clkb [remove_from_collection [all_clocks] $clka] {
        if {![string equal [string trimleft [get_obj $clka] "virtual_"] [string trimleft [get_obj $clkb] "virtual_"]]} {
            set period_clka [get_attr $clka period]
            set period_clkb [get_attr $clkb period]
            set value [expr [lindex [lsort [list $period_clka $period_clkb ]] 0] - ${MAX_DELAY_BUDGET}]
            if {[string match "virtual_*" [get_obj $clka]]} {
                set value [expr $value + ${IO_DELAY_RATIO}*$period_clka]
            }
            if {[string match "virtual_*" [get_obj $clkb]]} {
                set value [expr $value + ${IO_DELAY_RATIO}*$period_clkb]
            }

            set cmd "set_max_delay -ignore_clock_latency $value -from \[get_clocks [get_obj $clka]\] -to \[get_clocks [get_obj $clkb]\]"
            puts $cmd
            eval $cmd
            set cmd "set_false_path -hold -from \[get_clocks [get_obj $clka]\] -to \[get_clocks [get_obj $clkb]\]"
            puts $cmd
            eval $cmd
```

```
55 # From /proj/xiangqiudong/sdc_verif/top.syn.sdc li
56 set_max_delay \
57   -from { clk_core } \
58   -to { clk_sys } \
59    1
60
61 # From /proj/xiangqiudong/sdc_verif/top.syn.sdc li
62 set_false_path \
63   -from { clk_core } \
64   -to { clk_sys } \
65   -hold
```

TCM Lint

- SDC Lint check results
  - cd fishtail_rtl_verification/setup
  - view_fishtail_result –Verdi
- RTL & Clock issue Flagged by TCM:
  - RTL-*
  - CLK-*
- If not fix:
  - Impact further SDC Lint/Verification
  - Impact Synthesis & STA QoR and Performance.

Setup Issues

Waive	Issues	Severity	Message Count
☐			
	Parser Issues		
	Design Issues		
☐	Traversing a timing arc completes a combinational loop. (RTL-035)		6

Clock Definition Issues

Waive	Clock Definition Issues	Severity	Message Count
☐			
☐	Clock is redundant. Its removal will have no impact on the way the design is constrained. (CLK-027)		1

CLK-027 (1 message)

Regular expression for waivers: (applies to strings inside quotes in message)

Select all Messages | Unselect all Messages

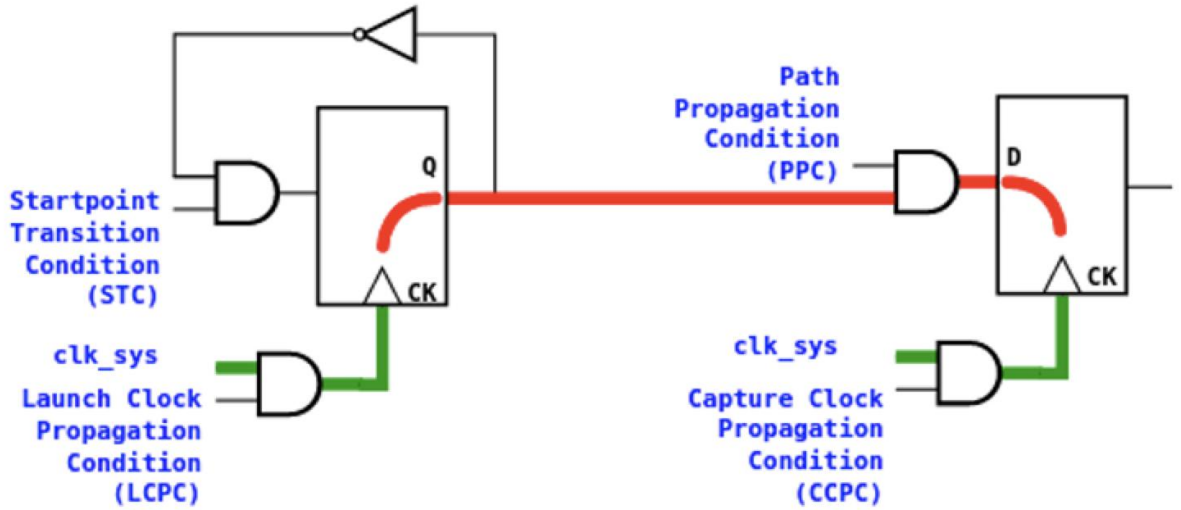
☐ Waive this message
Warning: Clock 'virtual_clk_core' is redundant. Its removal will have no impact on the way the design is constrained. (CLK-027)

```
# Virual Clock Define
create_clock -name "virtual_clk_core"    -period ${PERIOD_CLK_CORE}
create_clock -name "virtual_clk_sys"     -period ${PERIOD_CLK_SYS}
create_clock -name "virtual_clk_cfg"     -period ${PERIOD_CLK_CFG}
```

TCM Verify MCP/FP

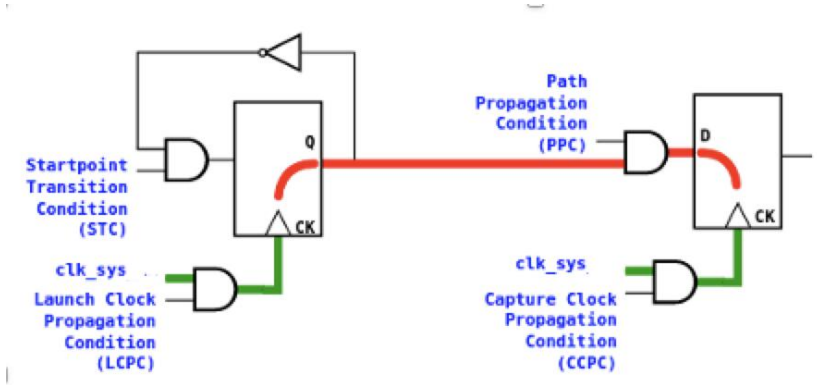
- **TCM structurally extract for MCP/FP on Sync Path**
  - STC: Start Point Transition Condition
  - LCPC: Launch Clock Propagation Condition
  - PPC: Path Propagation Condition
  - CCPC: Capture Clock Propagation Condition
- **TCM Formal engine Verify:**
  - STC/LCPC/PPC/CCPC relationship
  - To see any exception make Early Capture happen

Startpoint: apb_cfg_inst/wr_reg_pe_ena_reg[1]
☐ The startpoint is static
Endpoint: clint_inst/clint0_reg
☐ Failures to this endpoint can be ignored
☐ Failures between this start/end pair can be ignored
☐ The endpoint is allowed to go metastable



TCM Verify MCP/FP

- **MCP set on Data Path**
  - **Known Incorrect MCP**
  - **Formally Proven as Failed** as the 'PPC' can be true in the next clock cycle of 'STC'.



☐ Ignore STC
☐ Ignore LCPC
☐ Ignore PPC
☐ Ignore CCPC

Failure State:(=)

The path is not multi-cycle because when the startpoint transition condition is true, then in the next clock cycle it is possible for the path propagation condition to also be true. As a result, a transition on the startpoint will propagate to the endpoint in the same clock cycle.

```
78 set_multicycle_path 3 -setup  -from apb_cfg_inst/wr_reg_pe_ena* -to  clint_inst/clint*
```

Start/Endpoint Pairs For Clock Crossing Launch Clock clk_sys Capture Clock clk_sys

Reverify	Startpoint	Static Startpoint ☐	Endpoint	Waived Endpoint ☐	Waived Start End Pair ☐	Status	I/O Impacted	Static	Incorrect shift
☒	apb_cfg_inst/wr_reg_pe_ena_reg[1]	☐	clint_inst/clint0_reg	☐	☐	☒			
☒	apb_cfg_inst/wr_reg_pe_ena_reg[1]	☐	clint_inst/clint1_reg	☐	☐	✗			
☒	apb_cfg_inst/wr_reg_pe_ena_reg[1]	☐	clint_inst/clint2_reg	☐	☐	✗			

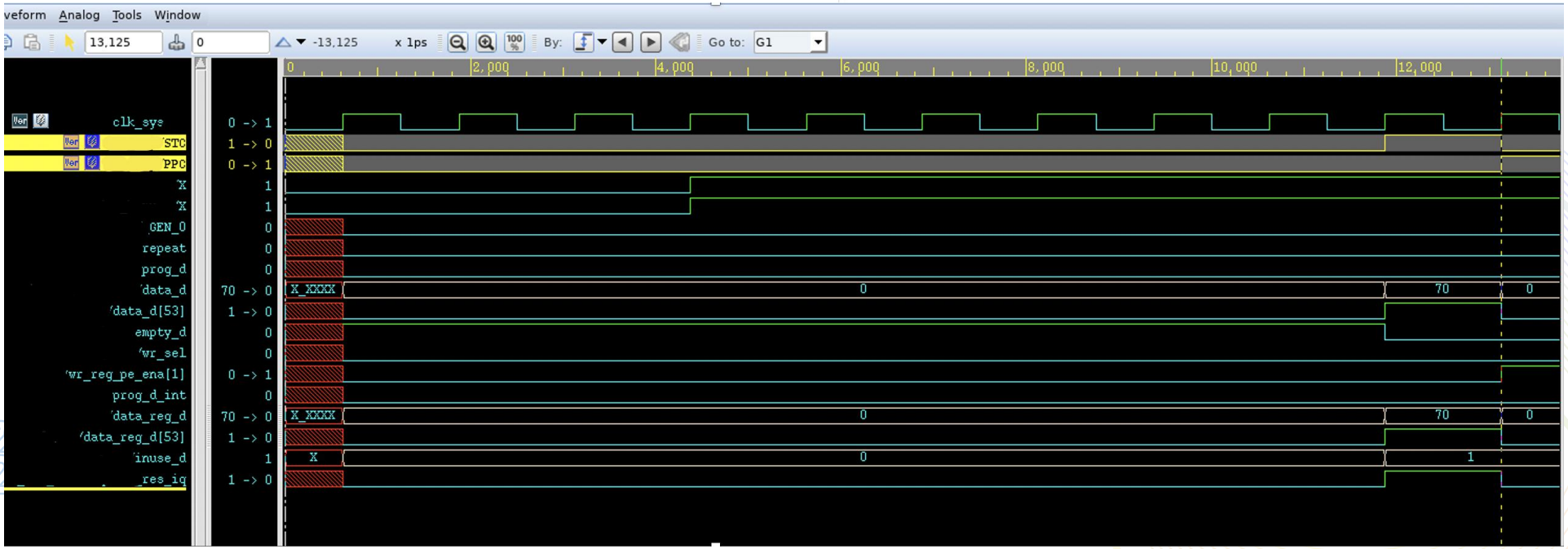
TCM Verify MCP/FP

- Steps to review Formal Result
  - ‘STC/LCPC/PPC/CCPC’ extracted by TCM
  - Waveform Generated by TCM Formal Engine
  - Check whether can apply Static/SCA?

Timing Path:

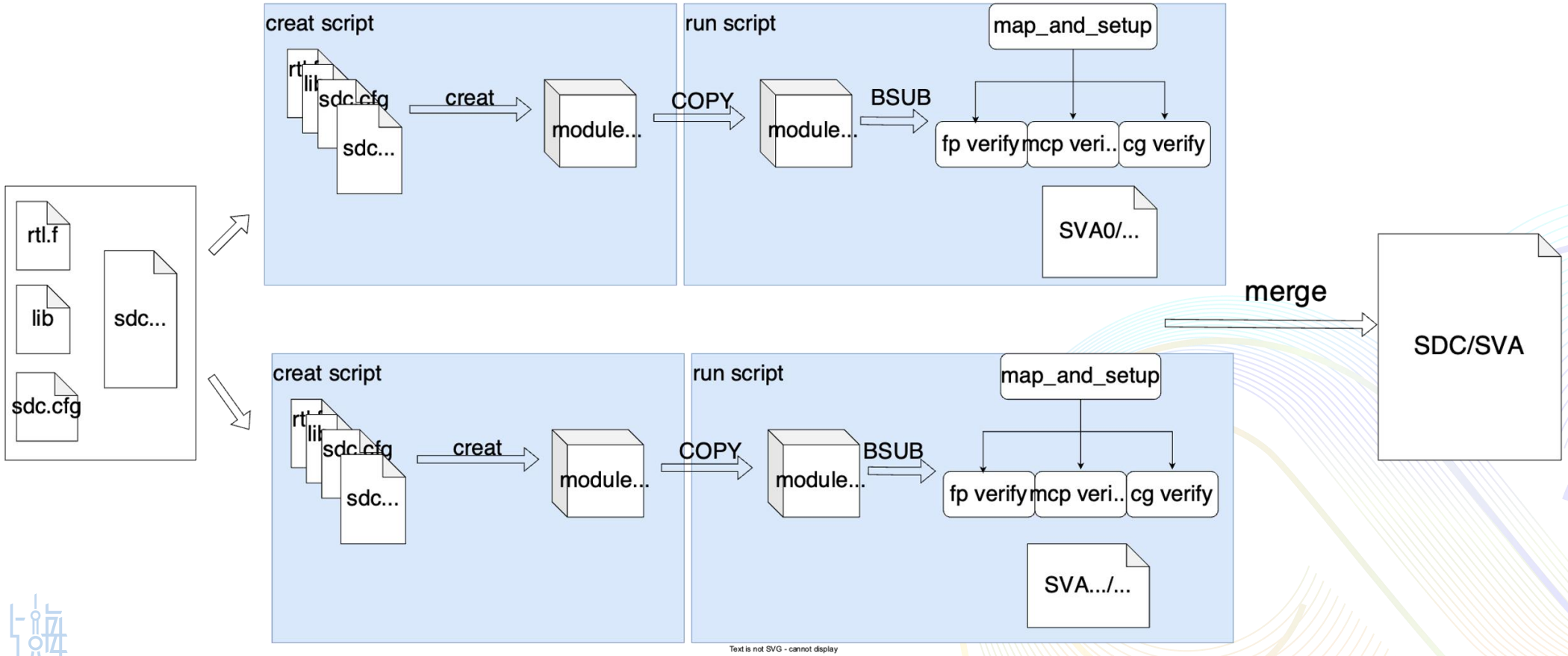
Hide Propagation Condition | Display Schematic

Timing Arc	Propagation Condition
apb_cfg_inst/ _clk(r)->apb_cfg_inst/wr_reg_pe_ena[1]	(1)
apb_cfg_inst/wr_reg_pe_ena[1]->apb_cfg_inst/clint_apb_wr_req	(1)
apb_cfg_inst/clint_apb_wr_req->apb_cfg_inst/clint_apb_wr_addr[*]	(1)
apb_cfg_inst/clint_apb_wr_addr[*]->clint_inst/clint_apb_wr_addr[*]	(1)
clint_inst/clint_apb_wr_addr[*]->clint_inst/apb_ipi_wr_sel[0]	**v1643129**
clint_inst/apb_ipi_wr_sel[0]->clint_inst/clint0_reg	**!v1643130**
clint_inst/clint0_reg->clint_inst/clk(r)	(1)



TCM verification

The Environmental Framework for TCM verification

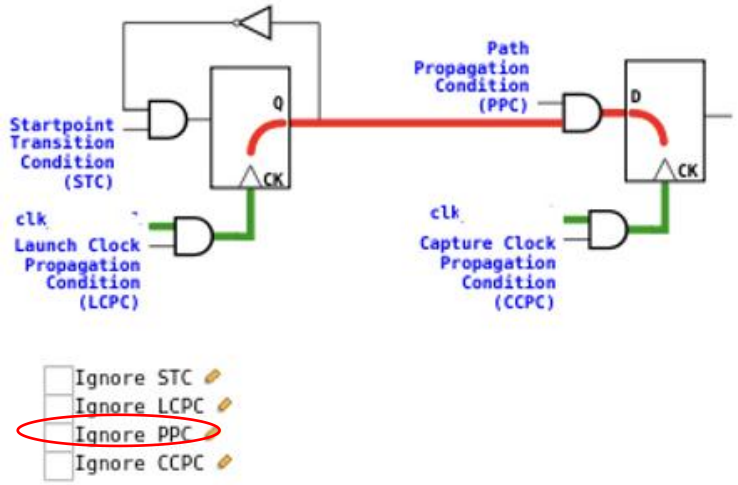


TCM verification

Comparison before and after mcp splitting

module	sdc number	paths number	memory	run time
test_all	10	>100000	>2.1T	>15days
test_0	2	11921	212G	~2days
test_1	2	22354	455G	~5days
test_2	2	55234	1T	~7days
test_3	2	22315	413G	~5days
test_4	2	11765	119G	~2days

TCM verification



Ignore ppc

Verification Results for 24 exceptions:

Classification	Exception Count	Path Count Formal	Pass	Fail	Total	Runtime
PASS	7	3001		0	3001	15:14
PARTIAL FAIL (Incorrect shift)	3	2290		18	2308	12:57
PARTIAL FAIL	2	8502		337	8839	2:16:46
NO PATHS	6					
PASS (MCP Hold < Setup)	6					

Total Passing Paths	13793
Total Failing Paths	355
Total Paths	14148
Passing path percentage	97%

Befor waive

Verification Results for 24 exceptions:

Classification	Exception Count	Path Count Formal	Pass	Fail	Total	Runtime
PASS	12	28490		0	28490	21:07
NO PATHS	6					
PASS (MCP Hold < Setup)	6					

Total Passing Paths	28490
Total Failing Paths	0
Total Paths	28490
Passing path percentage	100%

After waive

TCM verification

- verify the MCP paths inside the IP separately from the MCP paths at the top level of the SoC or the top level of the partitio
- Empty module or set module as black box
- Skip some steps

……

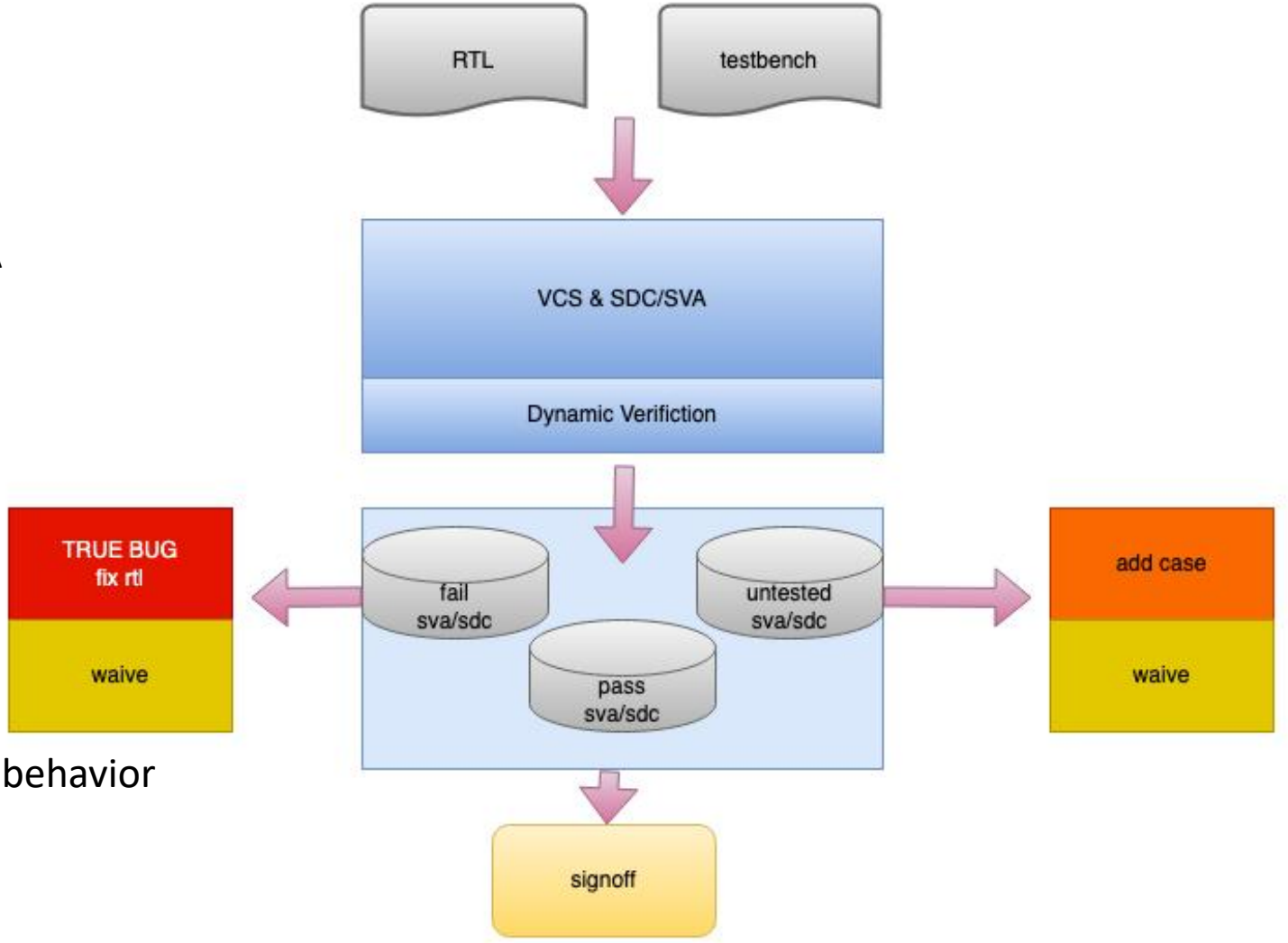
VCS With SDC/SVA Simulation Flow

Solution Overview

- Read SDC files during RTL verification

- Model timing uncertainty of waived paths in STA
  - Multi-Cycle Paths, False Paths
  - Two dynamic validation modes:
    - X-injection
    - Violation Checkers

- Advanced Features
  - Cross-check SDC declarations with simulation behavior



VCS SDC RTL Simulation Result

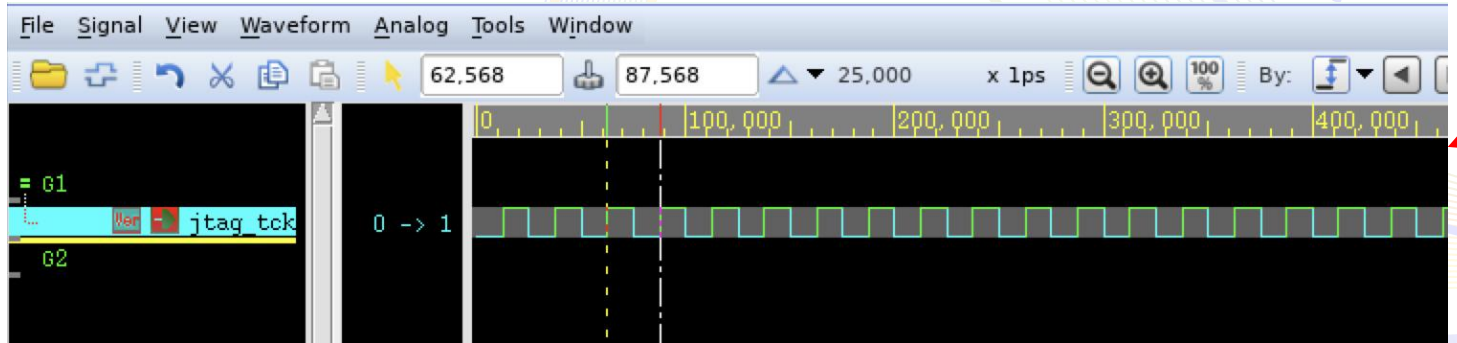
Sanity Check for Clock & SCA

- Issues Flagged by VCS-SDC:
  - set_case_analysis mismatch
  - clock Period mismatch

```
130 set_case_analysis 0 [get_pins "${CORE_TOP_HIER}basic_regfile_inst/sasrl_1p_test1_reg/Q"]
131 set_case_analysis 0 [get_pins "${CORE_TOP_HIER}basic_regfile_inst/sasrl_1p_test_rnm_reg/Q"]
132 set_case_analysis 0 [get_pins "${CORE_TOP_HIER}basic_regfile_inst/sasrl_1p_rme_reg/Q"]
133 set_case_analysis 0 [get_pins "${CORE_TOP_HIER}basic_regfile_inst/sasul_rm_reg_3_/Q"]
134 set_case_analysis 0 [get_pins "${CORE_TOP_HIER}basic_regfile_inst/sasul_rm_reg_2_/Q"]
135 set_case_analysis 1 [get_pins "${CORE_TOP_HIER}basic_regfile_inst/sasul_rm_reg_1_/Q"]
136 set_case_analysis 0 [get_pins "${CORE_TOP_HIER}basic_regfile_inst/sasul_rm_reg_0_/Q"]
137 set_case_analysis 0 [get_pins "${CORE_TOP_HIER}basic_regfile_inst/sasul_rme_reg/Q"]
```

```
SDC-ERROR: @ time 0 ps : set_case_analysis regfile_inst.sasul_rm[2], expected value 0 got 1
SDC-ERROR: @ time 0 ps : set_case_analysis regfile_inst.sasul_rm[1], expected value 1 got 0
```

```
SDC-ERROR:PERIOD @ time 62568 ps : clock dut.jtag_tck(clk_jtag), Observed: 25000 ps Expected: 20000 ps
SDC-ERROR:PERIOD @ time 87568 ps : clock dut.jtag_tck(clk_jtag), Observed: 25000 ps Expected: 20000 ps
```

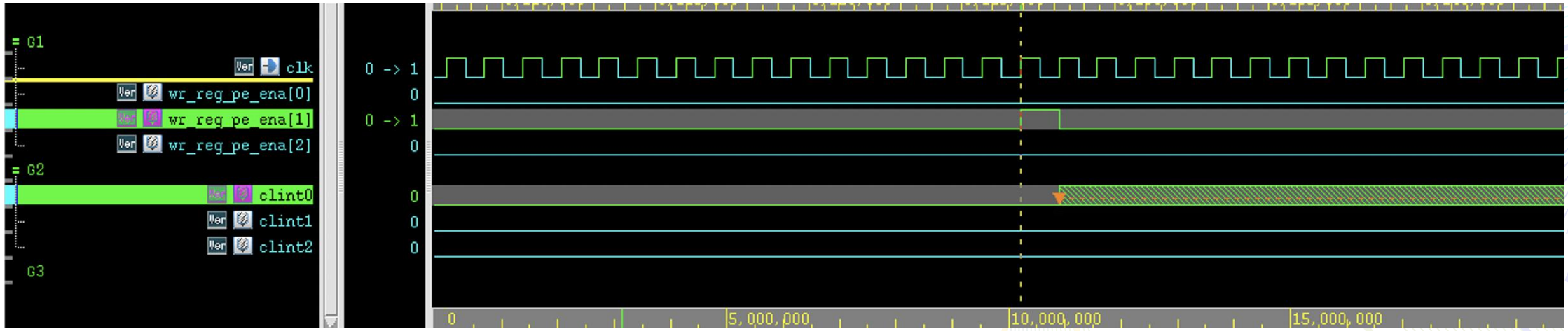


- Next Step
  - Review Design/SDC/Testbench
  - Fix Mismatch

VCS SDC RTL Simulation Result

```
[1] [MCP]-EARLY-CAPTURE-VIOLATION @ Time: 3215713 ps. TO clint_inst.clint0 (Clock: fishtail_rtl_verification/VCS_SDC_with_TCM/clock.mapped.sdc:12))
    |--> FROM apb_cfg_inst.wr_reg_pe_ena (Clock: cluster_clk (clk_sys:fishtail_rtl_verification/VCS_SDC_with_TCM/clock.mapped.sdc:12))
    changed @ Time: 3214463 ps. Observed 1 cycle delay, expected 3 cycle delay (set_multicycle_path fishtail_rtl_verification/VCS_SDC_with_TCM/mcp_fail.sdc:25)

UVM_ERROR @ 3268832: Description: Monitor Check for X or Z on PRDATA
UVM_ERROR @ 3268832: Description: Monitor Check for X or Z on PRDATA
```

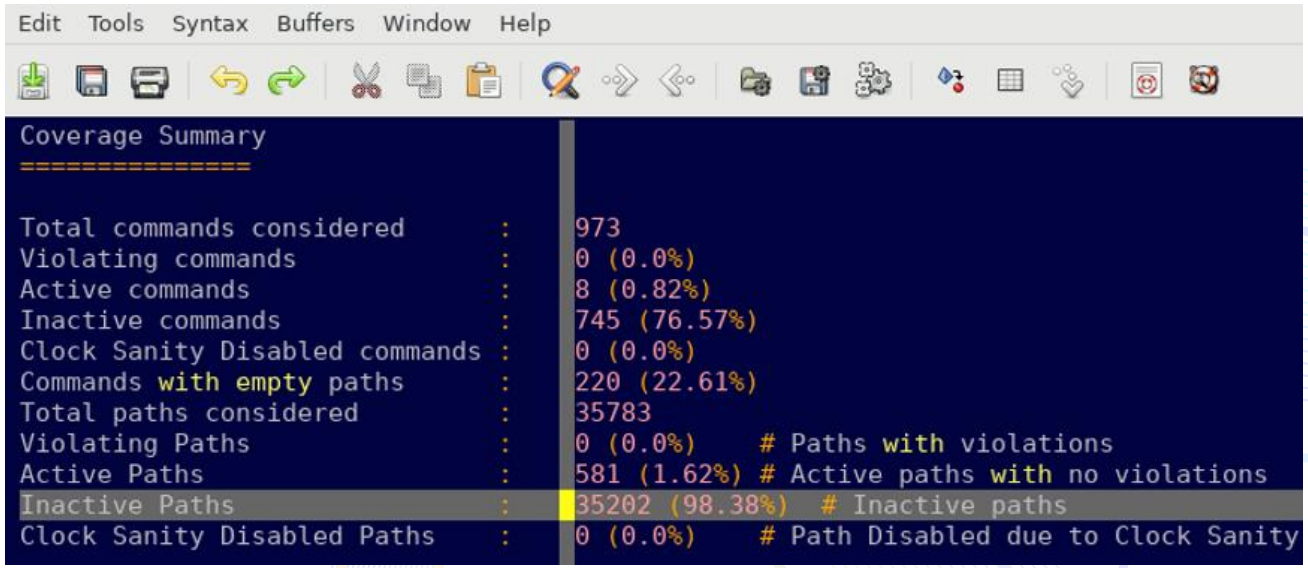


X-Injection happens as Early Capture on MCP Path and Leads to Simulation Fatal Issue

VCS SDC RTL Simulation Result

MCP/FP Coverage

- SDC coverage
- Total Path/violationg Path/Active Path/Inactive Path
  - **Next step Suggestion:**
    - Enhance testcase Coverage
    - Review TCM Formal Verification Result



VCS SVA RTL Simulation Result

SVA coverage result

	NUMBER	PERCENT
Total Number	523944	100.00
Uncovered	122609	23.40
Success	401335	76.60
Failure	290	0.06
Incomplete	8	0.01
Without Attempts	59	0.01

CONCLUSION

Different SDC issues caught by different Steps

Formal Constraint Lint

- TCM
- MCP
  - Missing Hold
- I/O
  - Missing Delay
  - Missing Drive/Load
- Clock
  - Redundant Define

Formal MCP/FP Verification

- TCM
- Original Correct SDC
  - 2 MCP on Reset Tree
    - 99% Proven Pass
    - **4 RTL BUGS**
  - MCP between Async
    - SKIPPED
- Distort False MCP/FP
  - 1 MCP & 1 FP
    - 100% Proven Fail

MCP/FP Dynamic Verification

- VCS SDC
- Original Correct SDC
  - set_case_analysis issue
    - Value mismatch
  - create_clock issue
    - Period mismatch
- Distort False MCP/FP
  - 1 MCP & 1 FP
    - Fail，early capture violation
    - Simulation fatal error

CONCLUSION

SDC Solutions Runtime Comparison

xxx_top	Runtime	Memory
VCS (POST-SIM)	160h	644G
VCS (RTL-Sim)	1h	15G
TCM SDC verification	12h	272G
VCS SDC	Elab: 13x of RTL-Sim Sim: 1.04x of RTL-Sim	3x of RTL-Sim

CONCLUSION

Shift-left：
Catch SDC Bugs Earlier, Win more time for RTL modification;

Shorten TAT to effectively verify SDC/RTL modifications before RTL Frozen.

Comprehensive：
TCM’s Formal Engine help to catch scenarios or corner cases which is not covered by Existing testcases.

Smarter POST-Sim:

Help to fine-tune Post-Sim priority

FUTURE WORK

- False path & group clock verifiction
- Sdc promotion flow
- *More efficient result statistics for sva&vcs verification*
- *Explore more methods for accelerating simulation*

……

2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA

accellera SYSTEMS INITIATIVE

Thank You !

16 Apr 2025 上海 SHANGHAI