2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA

accellera SYSTEMS INITIATIVE

Approaching Zero DPPM with Functional and Test Coverage Patterns Combined Methodology

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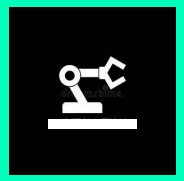
Agenda

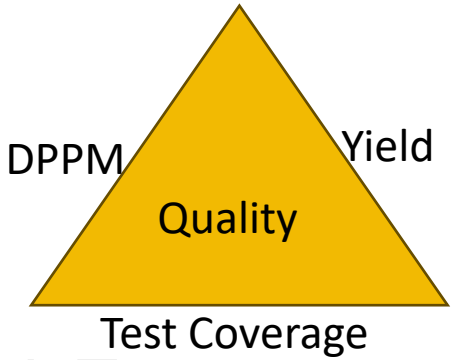
- Challenges of Achieving Zero Defects Parts per Million
- Challenges for Traditional ATPG Methodologies
- Proposed Functional and Test Coverage Patterns Combined Methodology
- Proposed DFT Flow
- Conclusions
- Q&A

Challenges of Achieving Zero DPPM

 **Assurance**	 **Exhaustive**	 **Automated**
Is coverage met for all fault models?	Do you have sufficient coverage to meet market requirements?	Is your flow automated and integrated for quick closure? And repeatable for future products?

Challenges of Achieving Zero DPPM （Cont.）

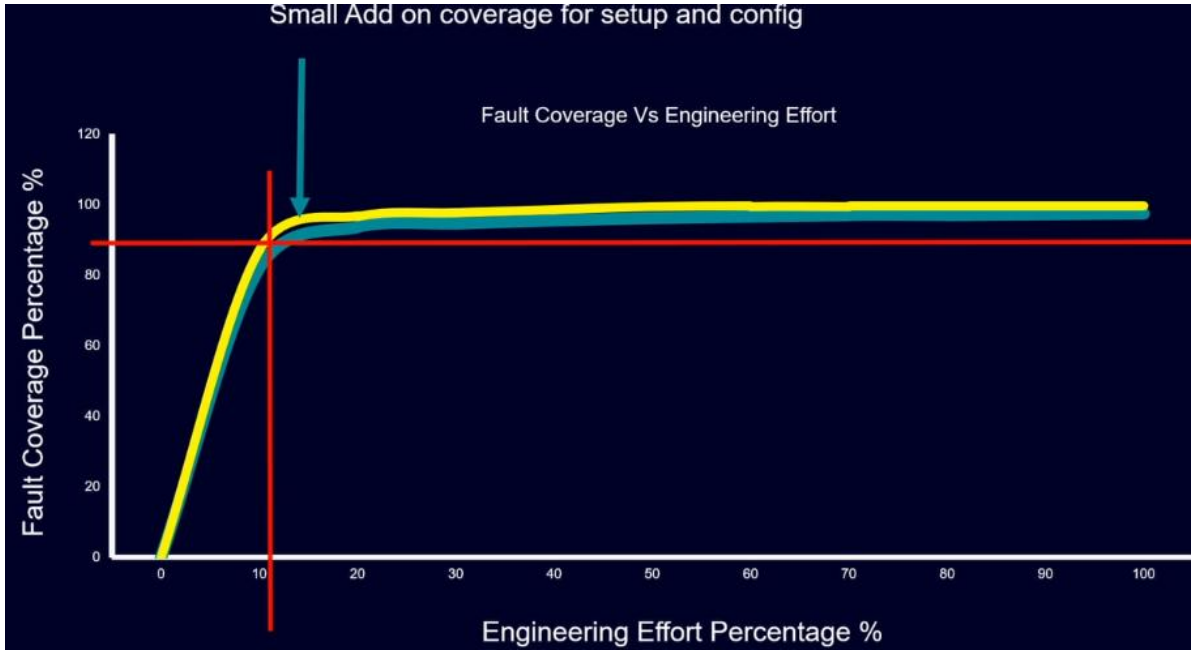
- Quality Triangle



- DL(Defect level) = $DL=1-Y^{(1-T)}$, Y: Yield, T:testcoverage
- DPPM=DL* 10^6

DPPM	Test Coverage	Supposed Yield
200	97.07%	99.32%
100	98.53%	
50	99.27%	
10	99.85%	

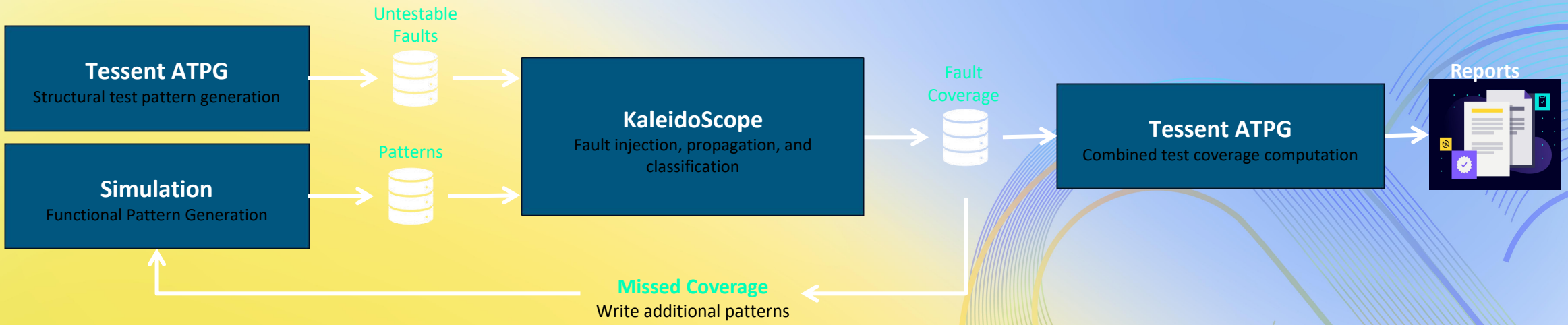
Challenges for Traditional ATPG Methodologies




```
1. Full (FU)
   1.1 TEstable (TE)
       a. DETEcted (DT)
          i.   DET_Simulation (DS)
          ii.  DET_Implication (DI)
          iii. DET_Robust (DR)—Path Delay Testing Only
          iv.  DET_Functional (DF)—Path Delay Testing Only
       b. POSDET (PD)
          i.  POSDET_Untestable (PU)
          ii. POSDET_Testable (PT)
       c. Atpg_untestable (AU)
       d. UNDetected (UD)
          i.  UNControlled (UC)
          ii. UNObserved (UO)
   1.2 UNTestable (UT)
       a. UNUsed (UU)
       b. TIed (TI)
       c. Blocked (BL)
       d. Redundant (RE)
```

- *Test_coverage= #DT + (#PD* posdet_credit) /(#FU -#UT)*

Augment test patterns with automated functional pattern coverage to achieve required coverage



Proposed DFT flow

- ***1. Tessent ATPG Structure Test*** to generates structural patterns
  - write_faults cpu_top_edt_stuck_stuck_basic.faults.mtfi -format mtfi -Replace -noeq -class AU -class PT -class PU -class UO -class UC -class RE -class TI -class BL -class UU.
  - write_ks_fdb -fusadb_name ./ Database/FaultGrade.fdb::TessentFaults
- ***2. Function level Simulation*** to generate functional patterns
  - Evaluate circuit operation at the function level
  - Detect functional issues missed by structural testing

Proposed DFT flow (Cont.)

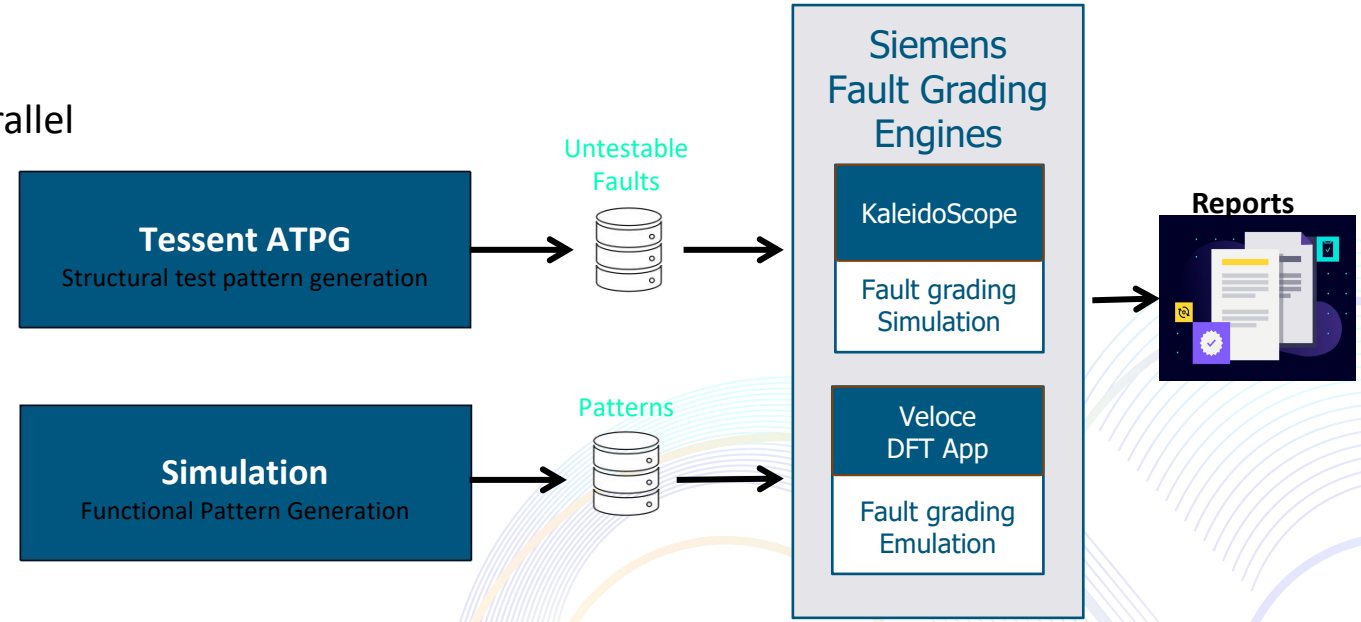
Complimentary fault engine solution – Utilizes strengths of simulation & emulation

Fault Simulation (concurrent)

- Advanced concurrent fault simulation of 1000s in parallel
- Best for IP/ block/subsystem simulations
- Native testbench (System Verilog, UVM)

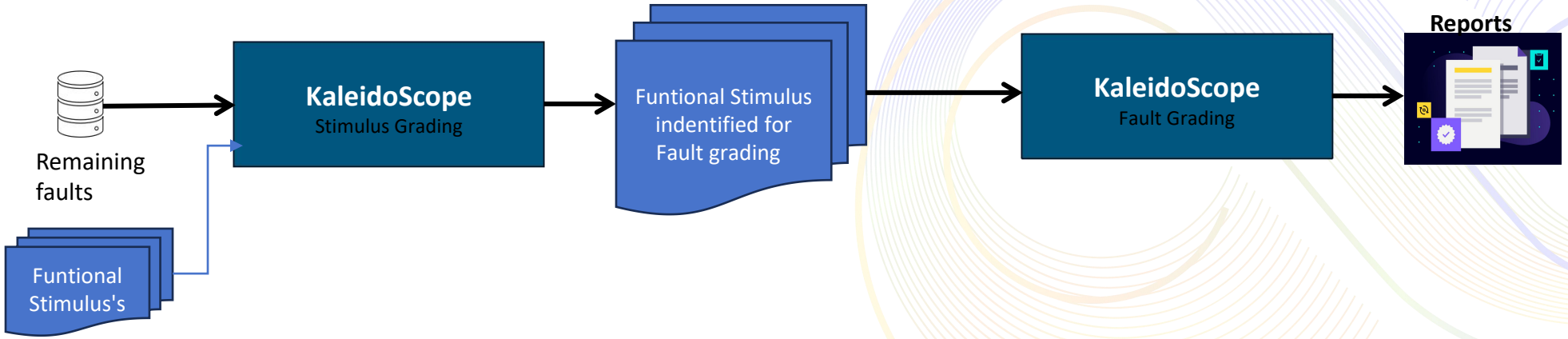
Fault Emulation (Fast)

- Fast serial fault simulation at 1000X speed
- Best for long SoC level simulations
- Tests requiring full SW stack
- Supports STIL format

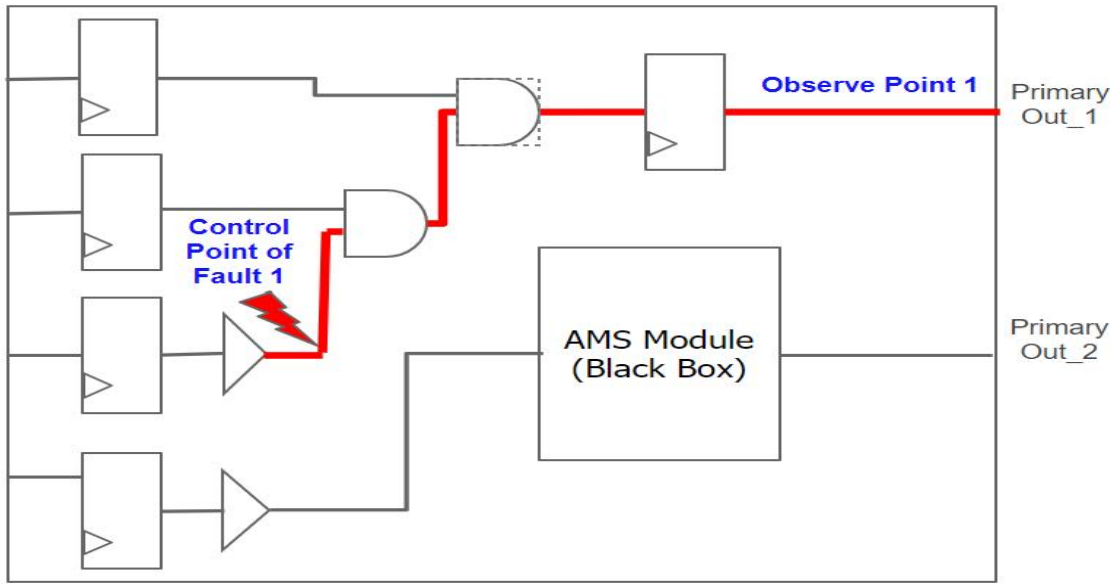


Proposed DFT flow (Cont.)

- ***3. Functional Fault Injection Simulation*** to evaluate how effectiveness of functional patterns to cover that faults that are not covered by ATPG patterns.
  - Step-1 : identify stimulus needed from full set of functional stimulus for given fault set
    - *rank them using the total faults that can be injected*
  - Step-2 : do actual fault grading using smaller set of stimulus



Proposed DFT flow (Cont.)



- ***Example run command of KaleidoScope***

```
KaleidoScope                                                    \
        --mode          kmanager_distributed                    \
        --kman_parallel    8                                    \
        --top           cpu_top                                 \
        --fusaini       ./Inputs/fusa.ini                       \
        --max_concurrent_fault 1000                             \
        --max_fanout       500000                               \
        --error_inject_inst cpu_top_cpu_top_stuck_chain_serial_v_ctl.cpu_top_inst  \
        --sim_qwave       ./Inputs/qwave.f                      \
        --ini           fault_db_name=./Database/FaultGrade.fdb::TessentFaults  \
        --ini           write_fusa_db=true                      \
        --ini           fusa_db_name=./Database/FaultGrade.fdb::KS_Results      \
        --ini           overwrite_session=true                  \
        --dft_observe_points  ./Inputs/observe_points.txt       \
        --output_dir      ./Outputs/stuck_chain_serial_qwave_db                 \
        --log_file        ./Logs/stuck_chain_serial_qwave_db.log
```

Proposed DFT flow (Cont.)

- ***4. Test Coverage Merge*** to improve test coverage
  - DS (det_simulation) faults increased from 224897 to 226407
  - 1510 faults detected with the functional testcase, 0.03% test coverage improvement
  - read_ks_fdb -fusadb_name ./Database/FaultGrade.fdb::KS_Results -fault_class DS

Fault Classes	Result after normal ATPG run		Results after merging the Austemper faults	
	#faults(total)	#faults(total relevant)	#faults(total)	#faults(total relevant)
FU (full)	298702	294271	298702	295719
UC (uncontrolled)	81 (0.03%)	same (0.03%)	53 (0.02%)	same (0.02%)
UO (unobserved)	19 (0.01%)	same (0.01%)	19 (0.01%)	same (0.01%)
DS (det_simulation)	224897 (75.29%)	same (76.43%)	226407 (75.80%)	same (76.56%)
DI (det_implication)	62081 (20.78%)	same (21.10%)	62081 (20.78%)	same (20.99%)
PU (posdet_untestable)	5 (0.00%)	same (0.00%)	5 (0.00%)	same (0.00%)
UU (unused)	4004 (1.34%)	same (1.36%)	4004 (1.34%)	same (1.35%)
TI (tied)	368 (0.12%)	same (0.13%)	368 (0.12%)	same (0.12%)
BL (blocked)	82 (0.03%)	same (0.03%)	82 (0.03%)	same (0.03%)
RE (redundant)	1348 (0.45%)	same (0.46%)	1348 (0.45%)	same (0.46%)
AU (atpg_untestable)	5817 (1.95%)	1386 (0.47%)	4335 (1.45%)	1352 (0.46%)
Test coverage	97.98%	99.48%	98.49%	99.51%

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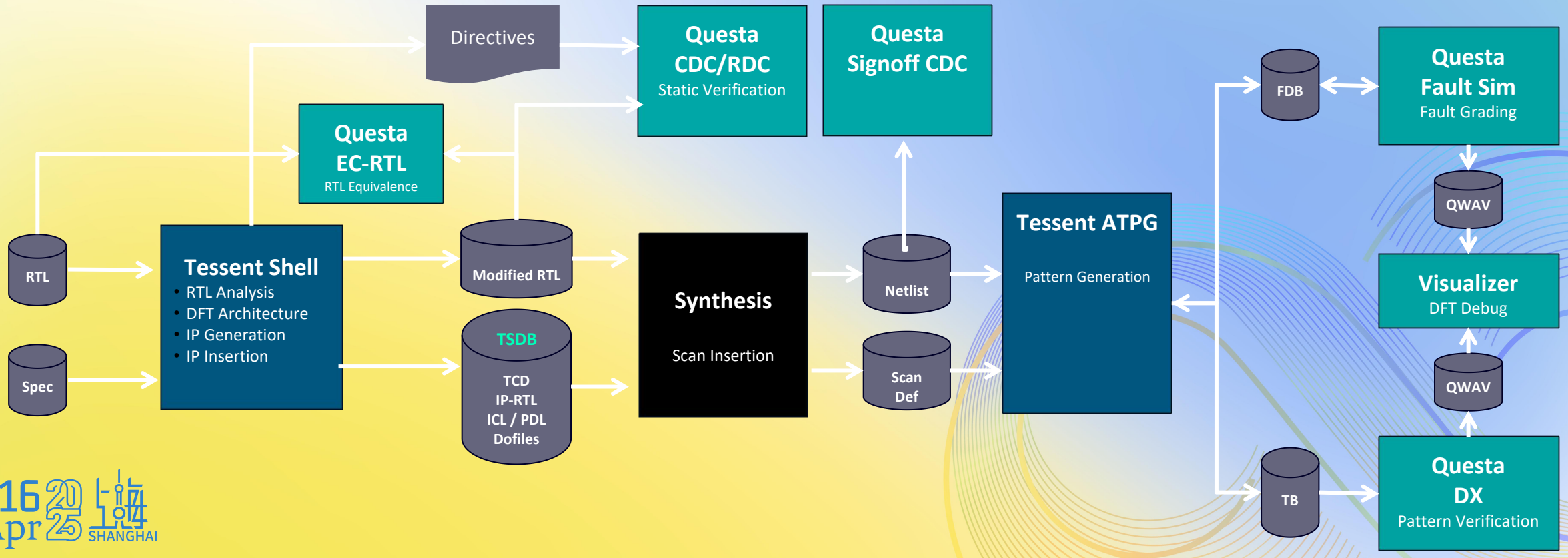
A comprehensive, high-productivity DFT verification solution



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More usages with Siemens EDA Questa Fault Sim

Fault Models

- Stuck-At, Transition delay
- Intra-Cell Bridge, Path delay, Cell-aware UDFM
- Roadmap (Inter-cell bridging, Opens)

Tessent Integration

- Reads Tessent reports to identify fault candidates
- Writes Tessent format for coverage merging
- Supports Tessent UDFM format

QFX with KaleidoScope Engine

Applications

- Functional pattern(s) coverage analysis
- Functional pattern optimization
- Burn-in coverage analysis

Performance and Features

- Concurrent Fault Simulation (Cores, Grid)
- Stimulus grading
- Good Machine Simulation w/ hierarchical support

Conclusions

- Innovative methodology integrates functional patterns with advanced test coverage strategies to enhance fault detection for low DPPM goals.
- New approach with only four steps.
  - Generate structural test patterns via Tessent ATPG and extract undetected faults in MTFI format.
  - Function level simulation to improve fault observability and propagation by leveraging high toggle rates stimulus.
  - Fault injection simulation with a parallel concurrent fault propagation engine of KaleidoScope for efficient functional fault grading and analysis.
  - Merge the existing coverage from ATPG and functional fault injection data by proactively addressing test coverage deficiencies early in the design phase
- A comprehensive, high-productivity DFT verification solution validated by Siemens EDA

Q&A