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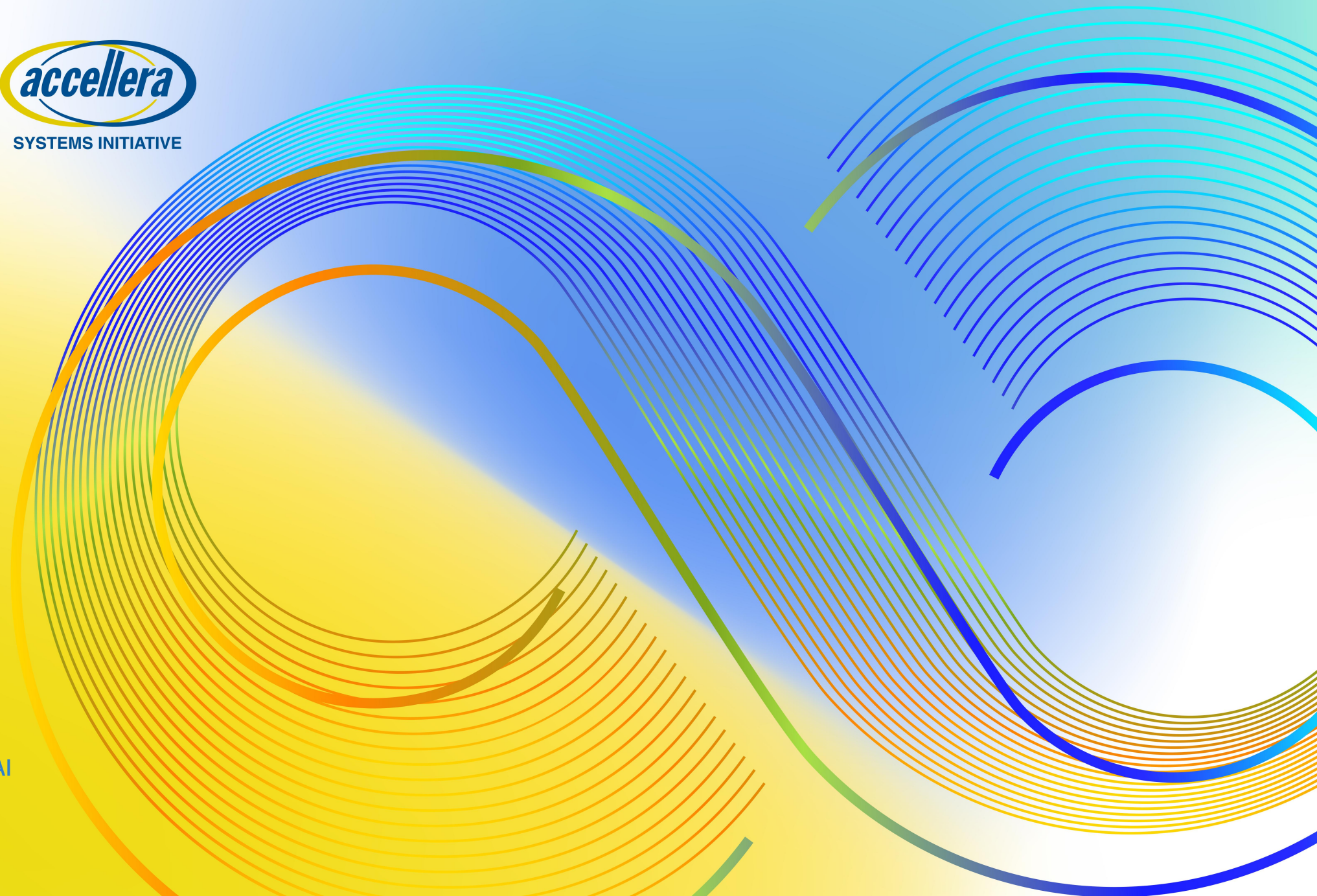
16 Apr 2025 上海 SHANGHAI



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A Practical High Level Verification Methodology for HLS design

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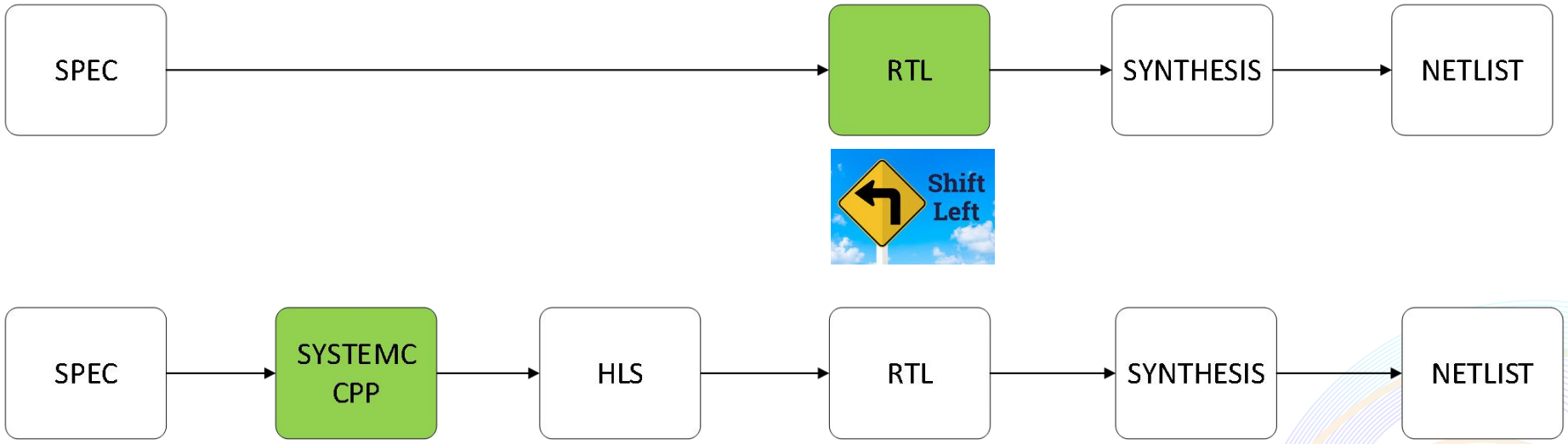
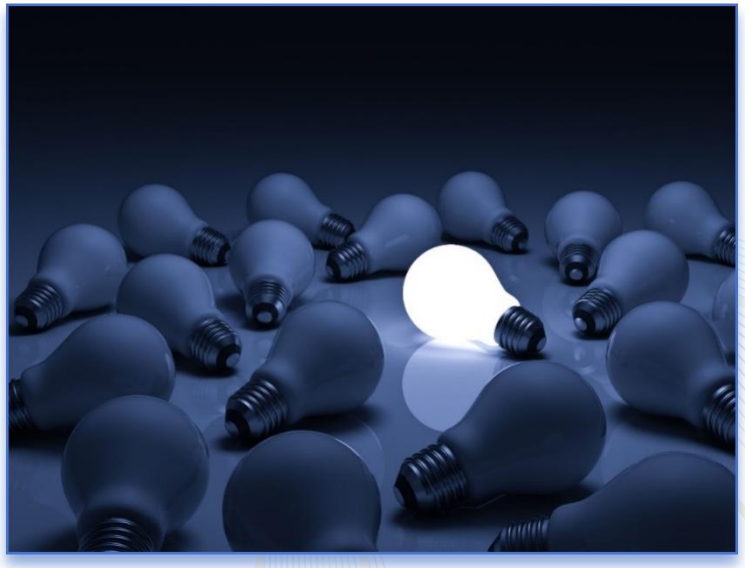
Verification of HLS



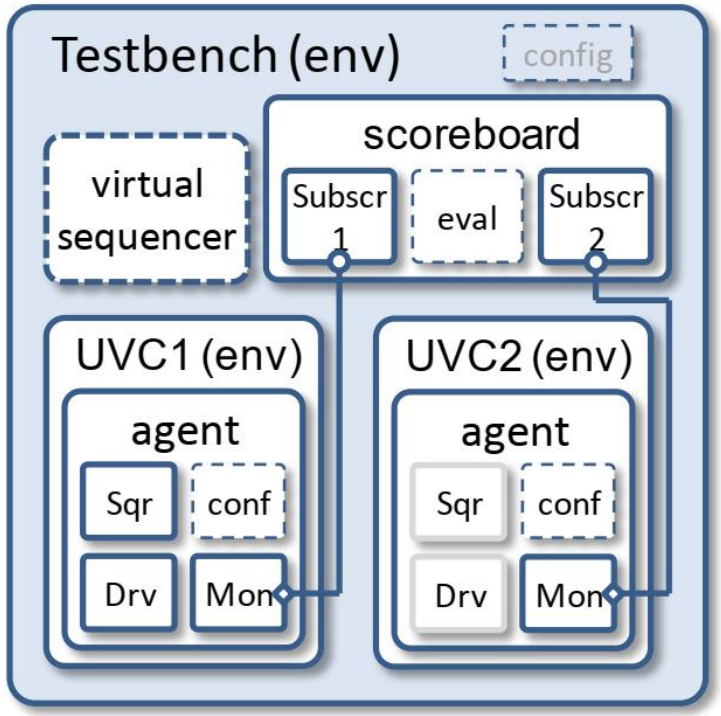
VERIFICATION CHANLLENGES using SYSTEMC

- UVM METHODOLY is developed in system-Verilog
- Constraint Randomization
- Register modeling
- Waveform dumping
- Verify CPP DUT by SYSTEMC TB
- RTL DUT simulation necessary?
- COVERAGE



UVM-SYSTEMC

UVM	UVM-SYSTEMC
Systemverilog	Systemc
Uvm_transaction	☑
Uvm_component	☑
Uvm_phase and object	☑
Config_db	☑
factory	☑
Field_automation	☒
Callback	☒
Register Abstraction Layer	☒



UVM-SYSTEMC library issues

- seq->start(env->vpi_slv->seqr) blocking later lines
- Solution: use config_db default_sequence

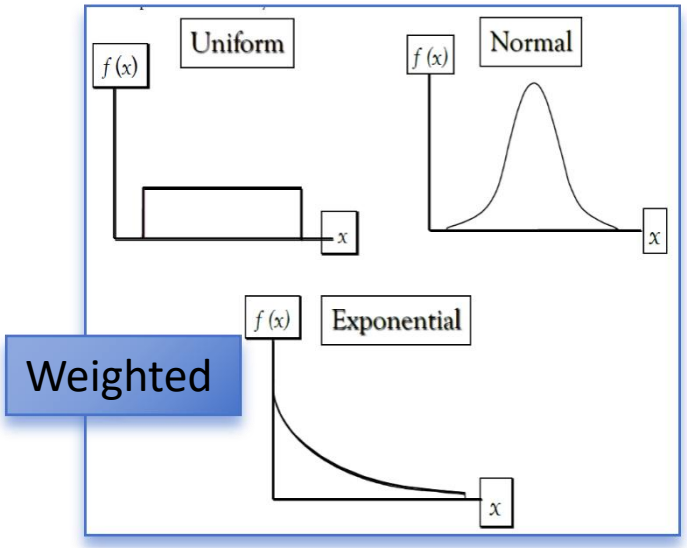
- Do not support uvm_analysis_imp_decl
- Solution:
  1. instantiate multiple uvm_subscriber in scoreboard
  2. Use function pointer

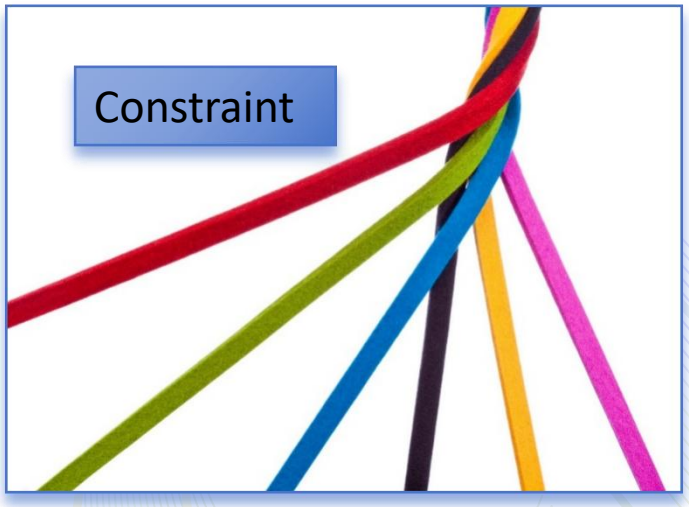
- No fork join_none in systemC
- Solution: Use sc_spawn launch dynamic thread

SCV

- SystemC Verification Libarary

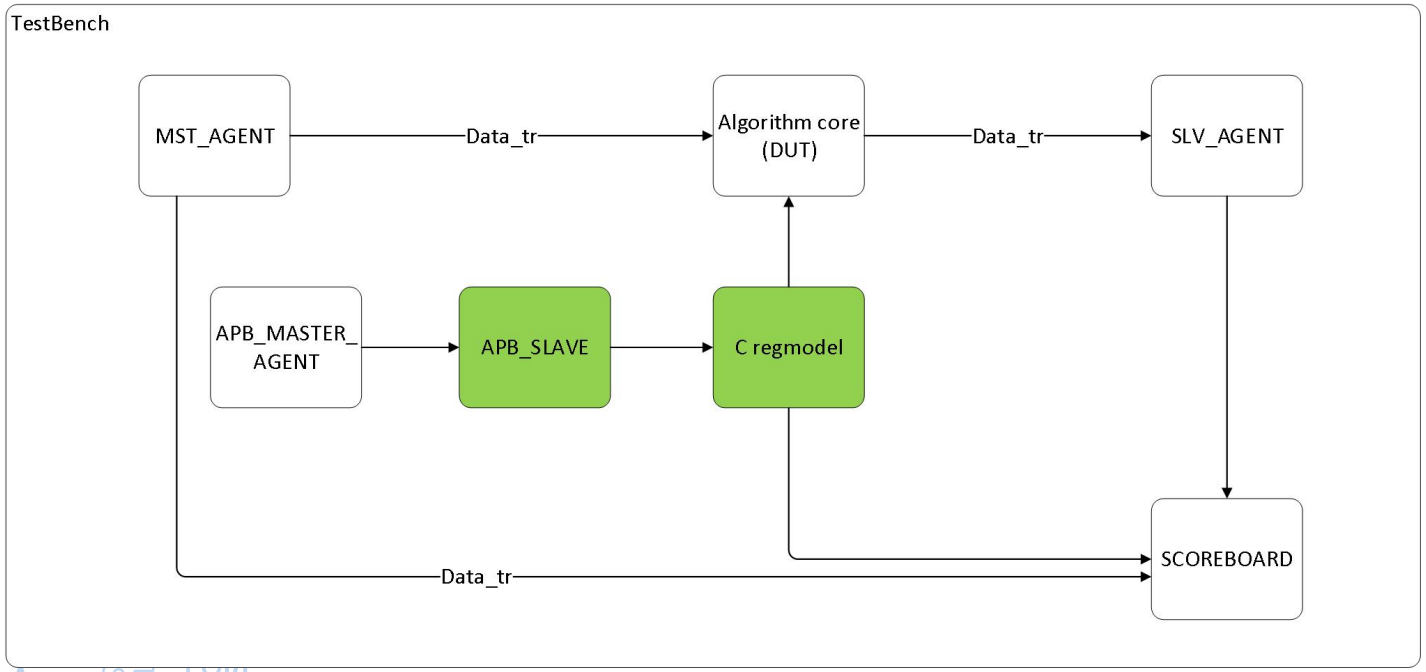
https://www.accellera.org/downloads/standards/systemc





C REGISTER MODEL

- E-SPEC generated C-REG
- Add APB_IF into C-register model

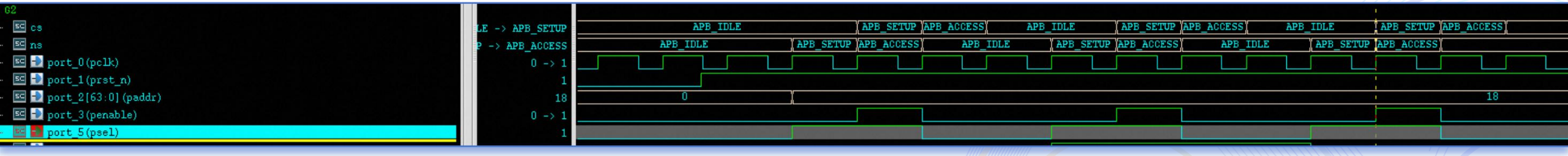


SYSTEMC WAVEFORM DUMPING

Sc_trace(trace_file_ptr,dut.clk,”dut.clk”);

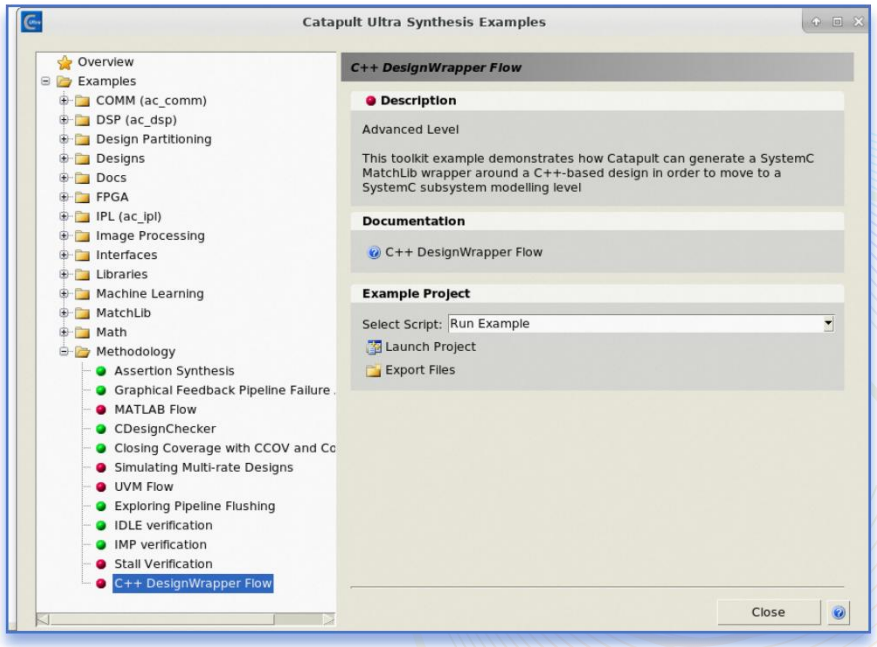
☒ $fdsbdumpvars

☑ VCS ucli: simv –ucli2Proc –ucli –do dump.tcl

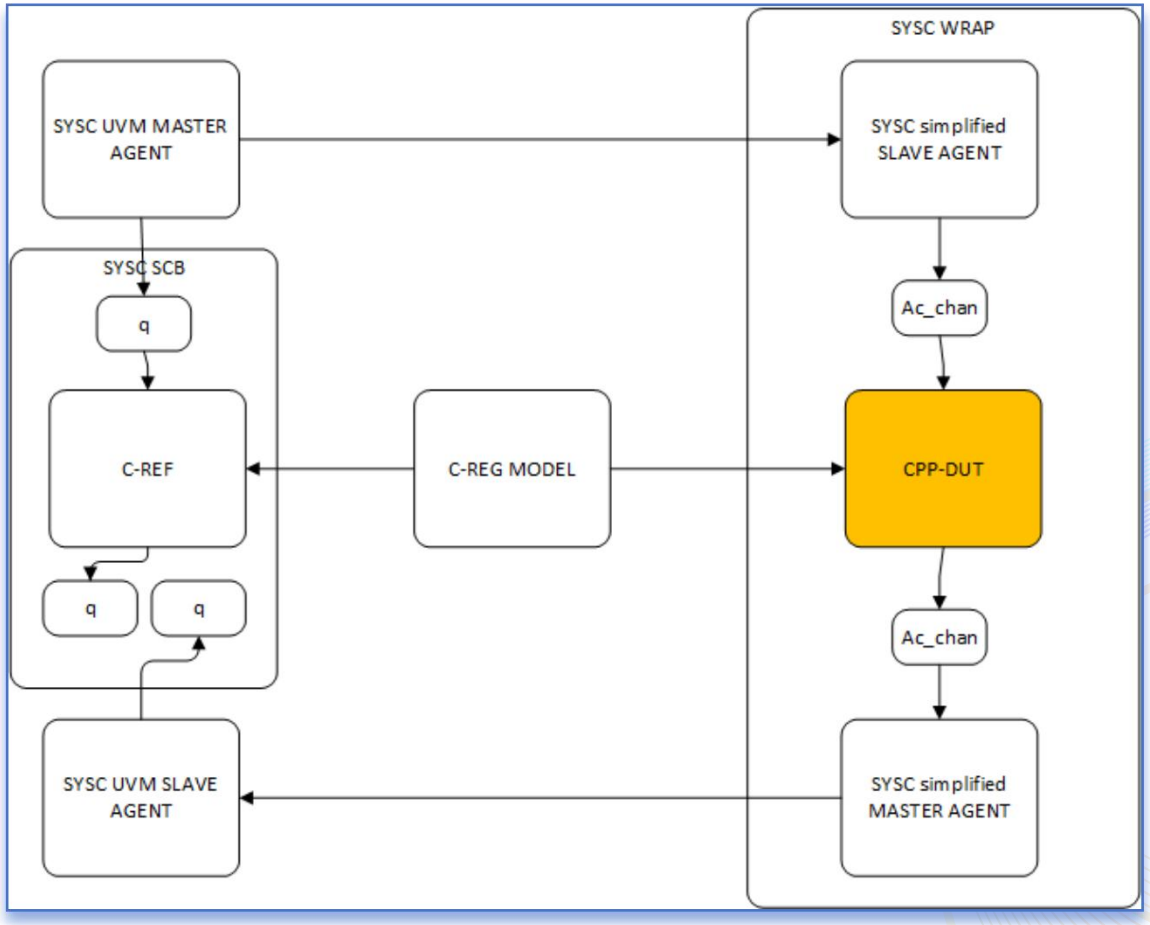


AUTO GEN CPP DUT SYSC WRAP

- Fill a common template to generate cpp top and systemC wrapper
- Write a script parse cpp top to generate systemC wrapper
- Use catapult C++ DesignWrapper Flow



SYSC WRAP FOR CPP DUT



HLS RTL DUT SIM

Reason to run RTL sim:

- Constraint/pragma check
- Performance evaluation
- C simulation is serial
- Check C->RTL

RTL DUT simulation method:

- SystemC TB with RTL DUT
- Re-use systemC cycle-accurate verification driver and monitor
- Use macro to sperate C/RTL tb lines
- Vlogan generate systemC wrapper for RTL DUT

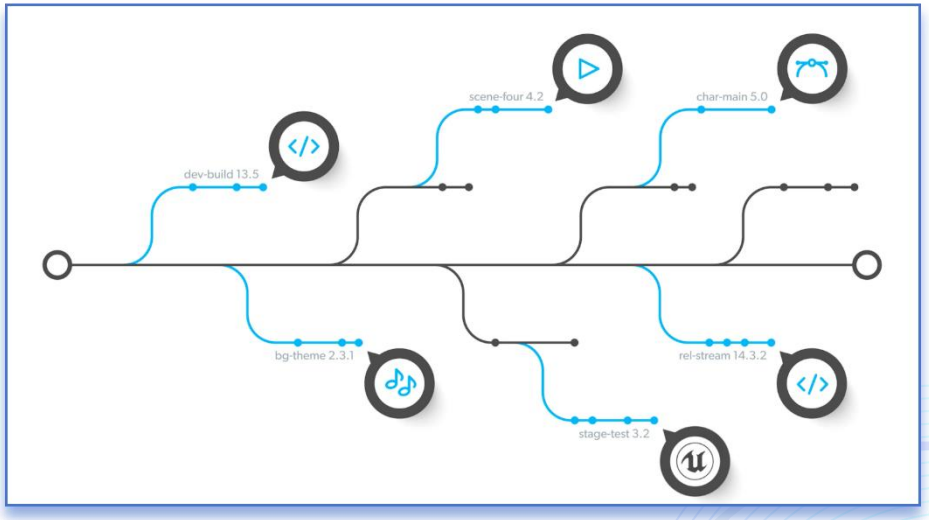
C COVERAGE

- CCOV: support C functional coverage and code coverage(toggle/line/branch)

INST MyCCoverGroup_5_inst	48.31%	0	100.00%	✓
CVP cp_a	100.00%	100	100.00%	✓
bin a_range_low	4	1	100.00%	✓
default bin a_default	0	-	-	✓
CVP cp_c_0	50.00%	100	50.00%	✓
CVP cp_d_0	1.56%	100	1.56%	✓
CVP cp_cnt	100.00%	100	100.00%	✓
CVP cp_out	33.33%	100	33.33%	✓
CROSS cross_cp_aXcp_c_0	33.33%	100	33.33%	✓
CROSS cross_cp_aXcp_cntXcp_out	20.00%	100	20.00%	✓

Summary of builds

- G++ build: basic build debug with gdb
- VCS build: waveform dumping
- CCOV build: for c functional and code coverage
- VCS C/RTL co-sim build: SYSTEMC-TB



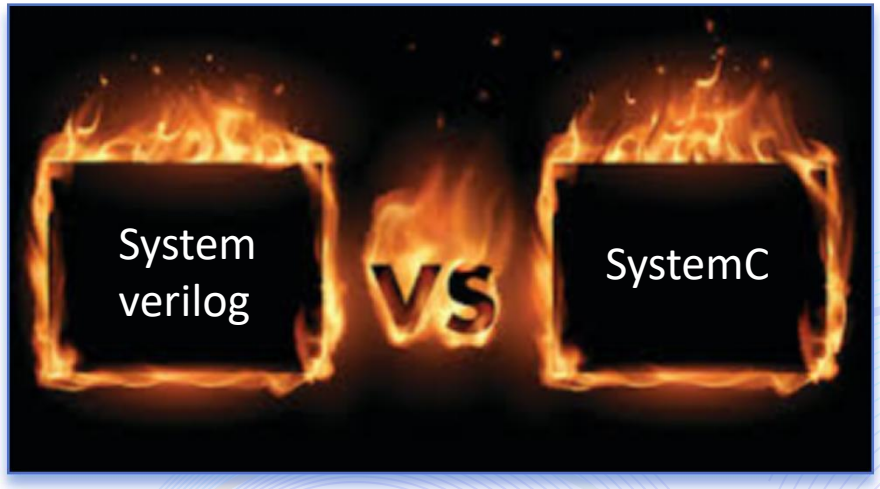
TOOL LIB VERSION

tools/library	version
g++	6.2.0_64
Systemc lib	2.3.2
Systemc-uvm lib	1.0-beta4
Systemc-verification lib(scv)	2.0.1
VCS	Q-2020.03-SP2
CCOV	2022.2
Catapult (HLS tool)	2022_1

Systemc VS systemverilog simulation

- SystemC simulation

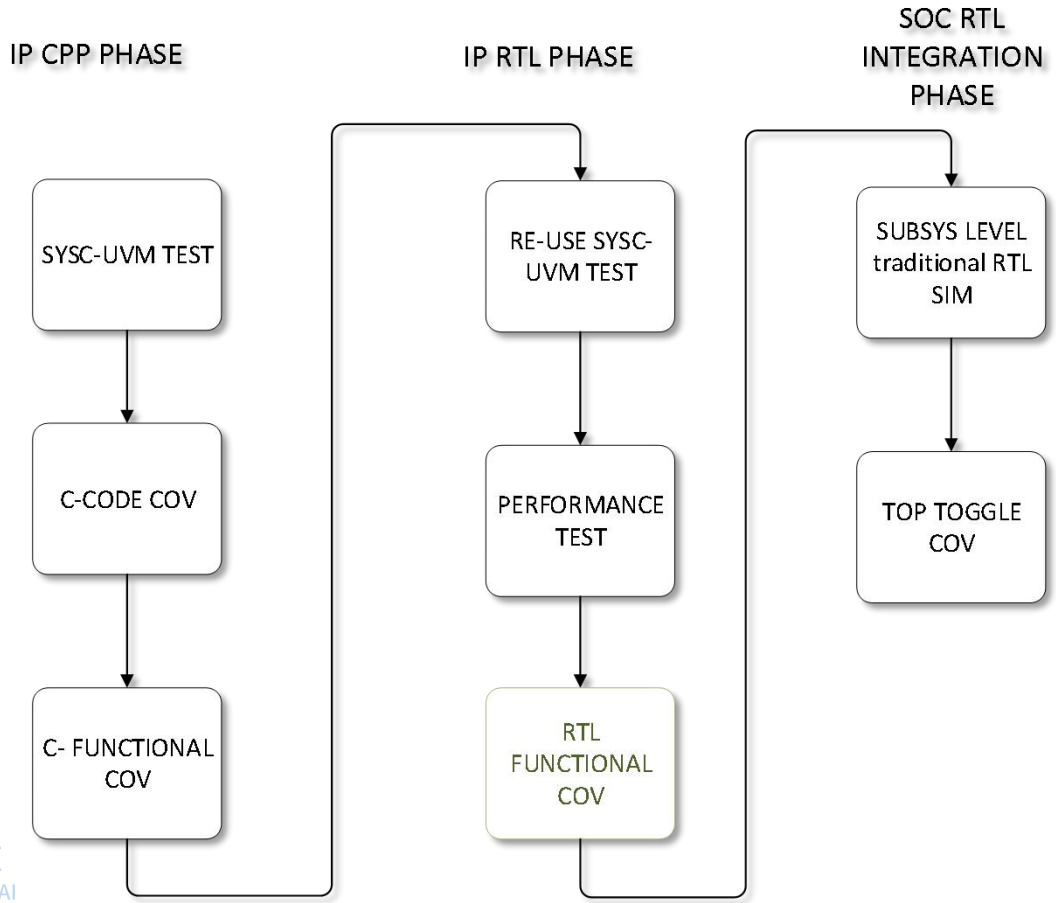
1. regression do not need license: use g++
2. less disk space
3. running faster 10X~100X
4. Support GDB debug except VCS/VERDI



- Systemverilog simulation

1. Methodology wildly accepted in industry
2. Lots of vendor VIP and testbench examples

HLS Verification flow summary



Final Summary

- Verification for HLS design
- Shift-left verification to C
- Introduced SystemC-UVM do verification
- Get C constrained randomization ability by SCV
- Solve C waveform dumping issue by VCS
- Re-use E-SPEC generated C-register model for verification
- Use CCOV to get C functional and code coverage
- Discussed SYSTEMC TB sim CPP DUT and RTL DUT

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THANK YOU

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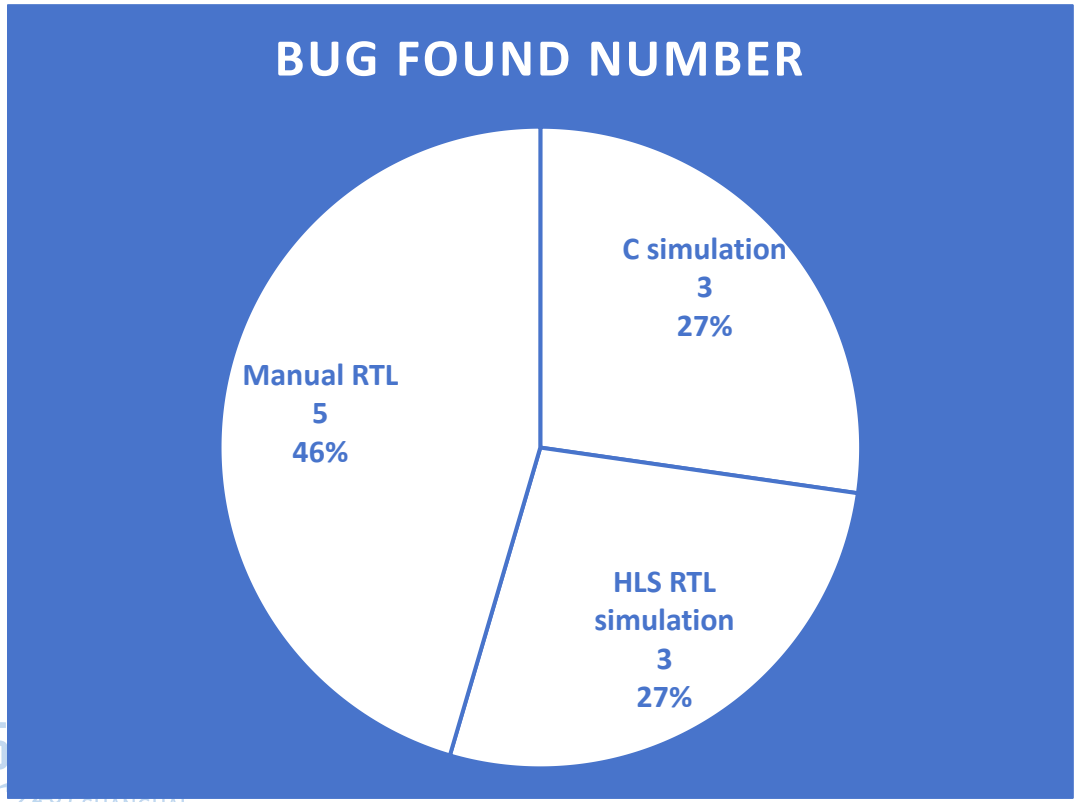
BUG FOUND

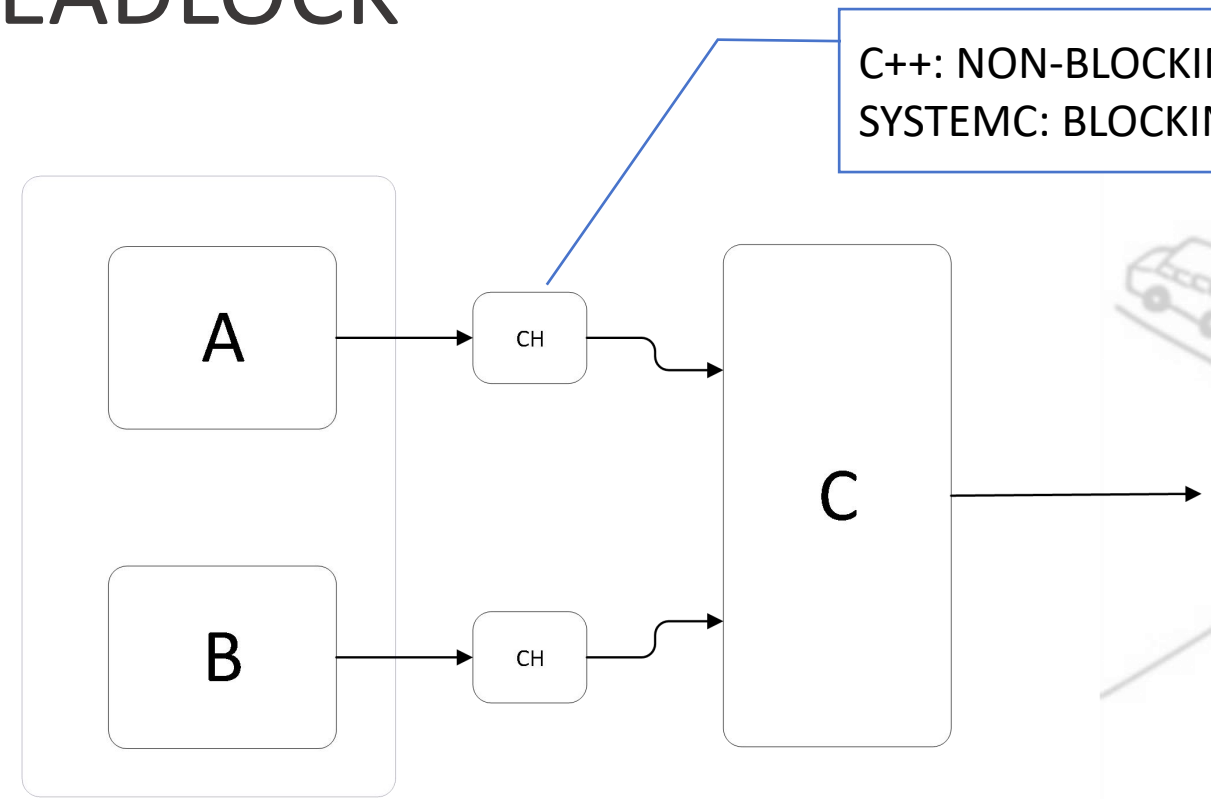


Total bug number: 14

3 typical bugs found in HLS RTL simulation:

1. Missing pragma
2. Deadlock
3. Performance

DEADLOCK

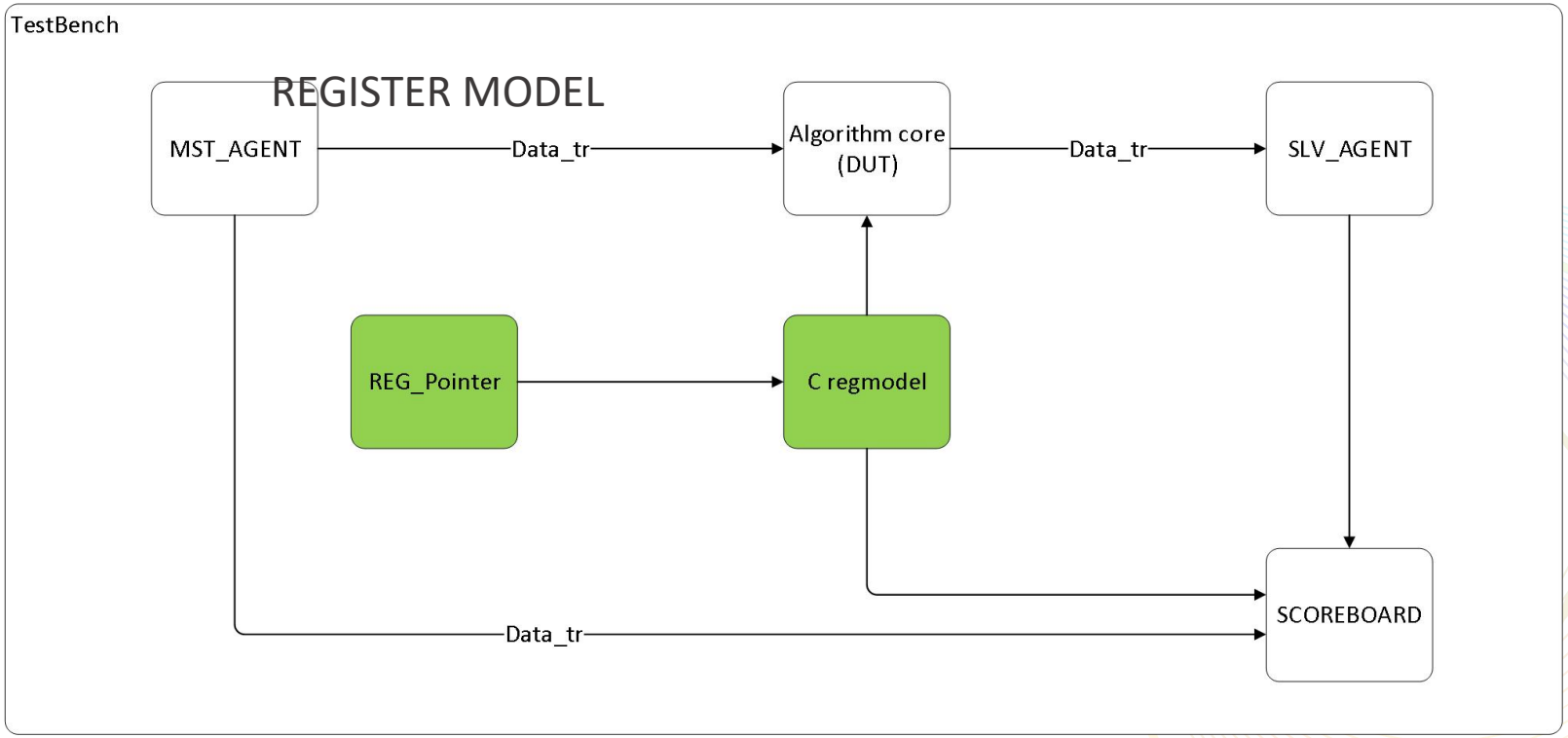


A/B transaction 1:1 generate

C = 4A+B

C REGISTER MODEL

- E-SPEC generated C-REG



Add APB_IF into C-register model