Agenda		Speaker
Workshop		
Harness Emulation and Prototyping to Customer Verification Efforts		
15:45-16:30	Harness Emulation and Prototyping to Customer Verification Efforts	Qinyi Liu Verification Consulting Engineer Director, XEPIC
Tutorial		
Advanced FusionVerify Platform for System-Level Verification		
16:30-17:00	• Empowering Designers with Efficient Equivalence Checking	Sera Gao Verification Consulting Engineer Director, XEPIC
17:00-17:15	XEPIC GalaxEC Demo	
17:15-17:50	• Unleashing Advanced Simulation Capabilities for IP and SoC Verification • Unleashing the Power of the Digital Verification Debug Platform	
17:50-18:00	Lucky Draw	

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扫码填写问卷

参与幸运抽奖!

1st Prize

2nd Prize

3rd Prize

2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA

accellera SYSTEMS INITIATIVE

Harness Emulation and Prototyping to Customer Verification Efforts

Qingyi Liu

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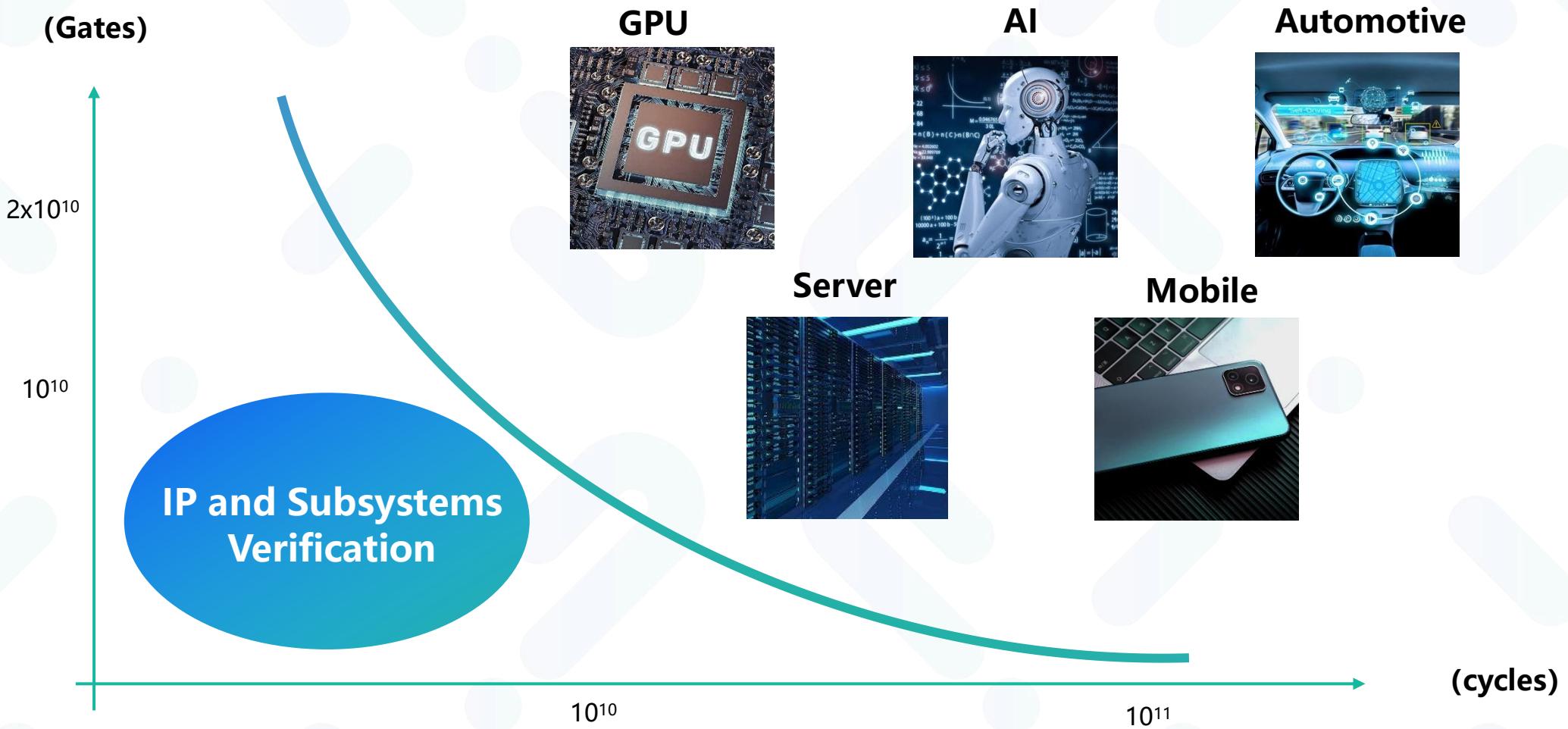
System Level Verification



Prototyping OR/AND Emulation

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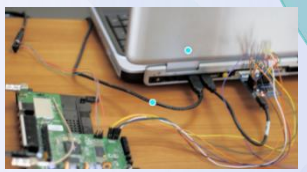
Prototyping

system validation

system prototyping



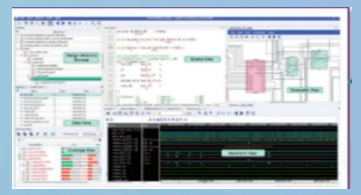
Software development

Emulation

Speed Bridge

Virtual Host Virtual Platform

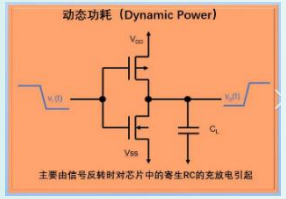
Transaction Base Acceleration



Debugging

Virtual Device

Performance



Power Analyze

Pressure testing

HuaPro And HuaEmu

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2021.11

HuaPro P1

High Performance FPGA-based Prototyping System

2022.12

HuaPro P2E

High-performance Dual Mode FPGA Verification System

2023.06

HuaEmu E1

High-performance Emulation System

HPE: HuaPro P2E & HuaEmu E1

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RTL synthesis

- High performance netlist generation
- Automatic Memory Module Recognition
- Full RTL signal naming mapping
- Incremental compilation logic resource optimization

Intelligent compiler

- Intelligent module detection
- Automatic Design Segmentation
- Automatic TDM Multiplexing IO
- Automatic connection topology generation
- Automatic modification of gated clocks
- No clock resource limitations
- Automatic conversion of memory implementations
- Automatic invocation of DPI connections Port Hybrid Emulation

Run-time Debugging

- Programmable Triggers (Trigger)
- Full-signal waveforms
- Automatic reference clock selection to capture multi-clock domain data
- Backdoor access
- Signal read/write and control

XEPIC unified Database

- RTL
- Netlist
- Log
- Waveform
- Coverage

Waveform Debugging

- Automatic waveform comparison
- Automatic source code and circuit correspondence
- Automatic signal tracing and fault analysis
- Automatic coverage statistics

➢ Complete, Autonomous Software Stack ➢ Unified database

Unified Front-end Parsing : GalaxSim

X-EPIC

Unified Verilog parsing tools

Normalized Input

Comprehensive tools dedicated to Emulation

Comprehensive syntax support

EEE1364 Verilog Standard

IEEE1800 SystemVerilog Standard

IEEE1800.2 UVM Standard

Automatic recognition and mapping

Automatic Memory Recognition

Automatic Clock Gate Recognition

Automatic memory model mapping

High Speed

Provide compilation performance

Ensure iteration efficiency

TBA

Supports TBA mode

Debug Database

Built-in Debug Database Supports Waveform to RTL Mapping

RTL Waveform Debugging

Unified Logic Synthesis Tools : vSyn

X-EPIC

vSyn provides the possibility to optimize the whole system to Prototyping and Emulation. In addition, vsyn also aligns the definition of the debug feature

Synthesis Tool for Emu

The only self-developed Synthesis tool specialized for Emulation

High Performance

Combined time is 10x longer than comparable products

Guaranteed iteration efficiency

Automatic recognition and mapping

Automatic Memory Recognition

Automatic Clock Gate Recognition

Automatic memory model mapping

Incremental compilation

Further improve compilation performance

Ensure iteration efficiency

Optimization

Logic Resource Optimization

Timing Optimization

Debug Database

Built-in Debug Database Supports Waveform to RTL Mapping

RTL Waveform Debugging

Sequential Equivalence Checking

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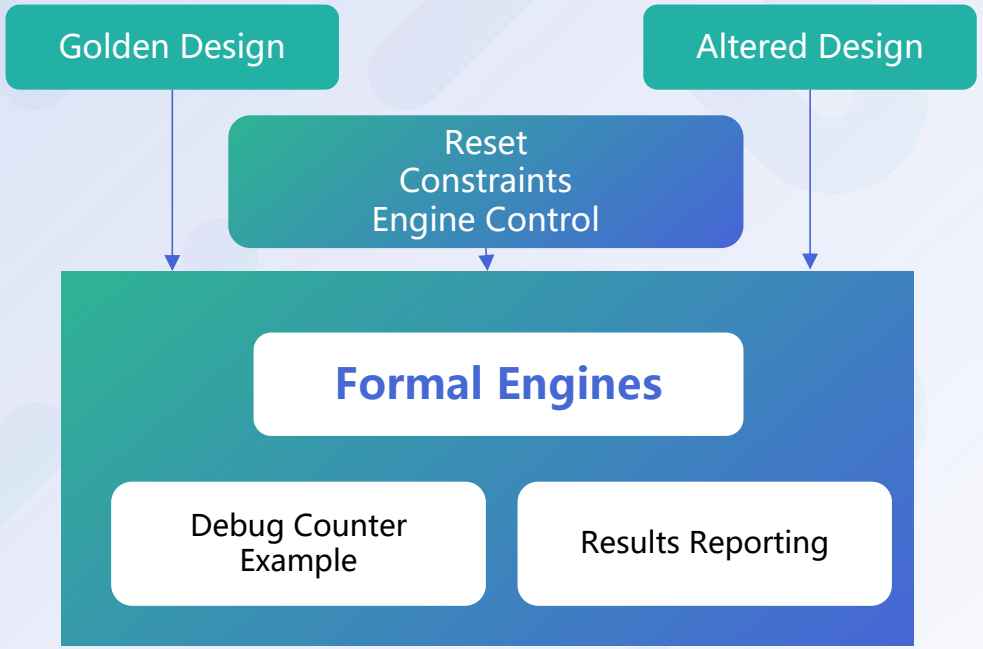
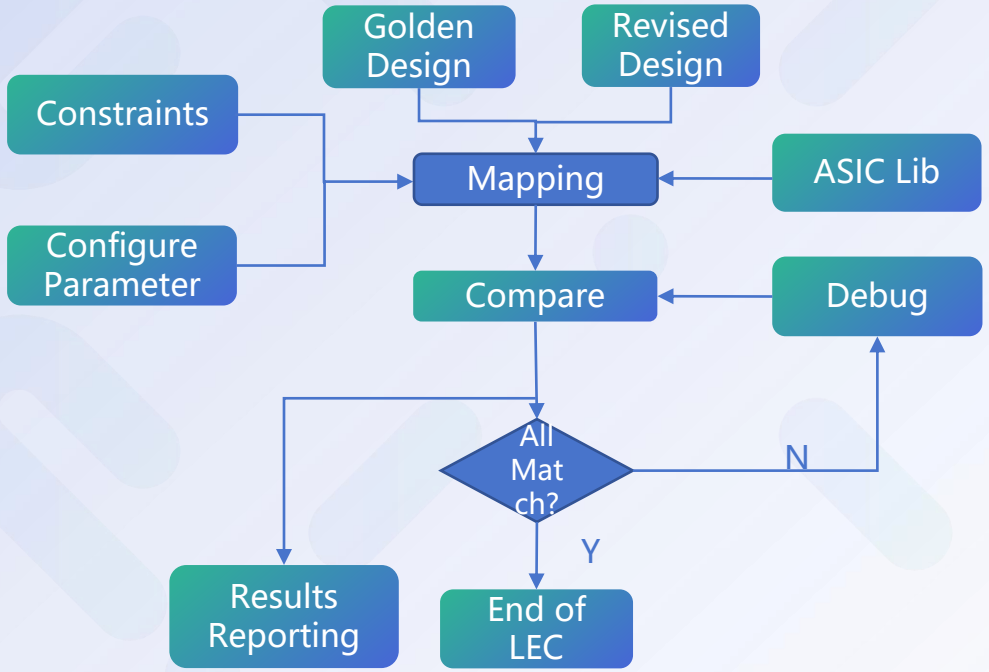
- **Sequential Equivalence Checking**



- **Logic Equivalence Checking**



Solution For Prototyping AND Emulation

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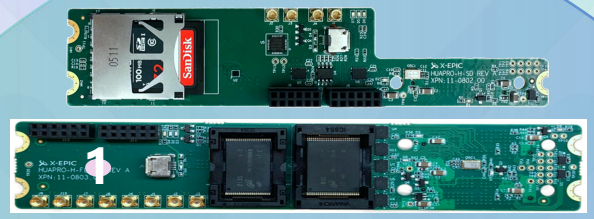
Prototyping

高速子卡：PCIE EP/RC / USB / Ethernet / MIPI

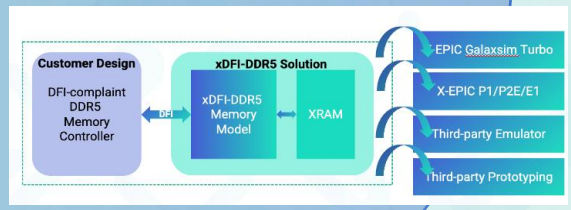
系统增强：Sram 子卡

Emulation

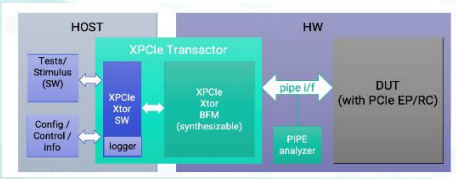


低速子卡：GPIO (UART / JTAG / CAN /IO)，SRAM，IOLAB，NAND Flash，NOR Flash，QSPI Flash，EEPROM，SDIO Card，DVP

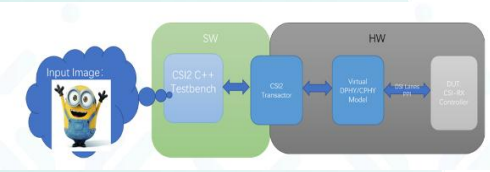
Speed Bridge：PCIe / USB / Ethernet



可综合模型：PCIE PHY / DDR4 / LPDDR4 / DDR5 / LPDDR5 /HBM



Virtual Link：
AXI / PCIe EP/ USB Device / Ethernet

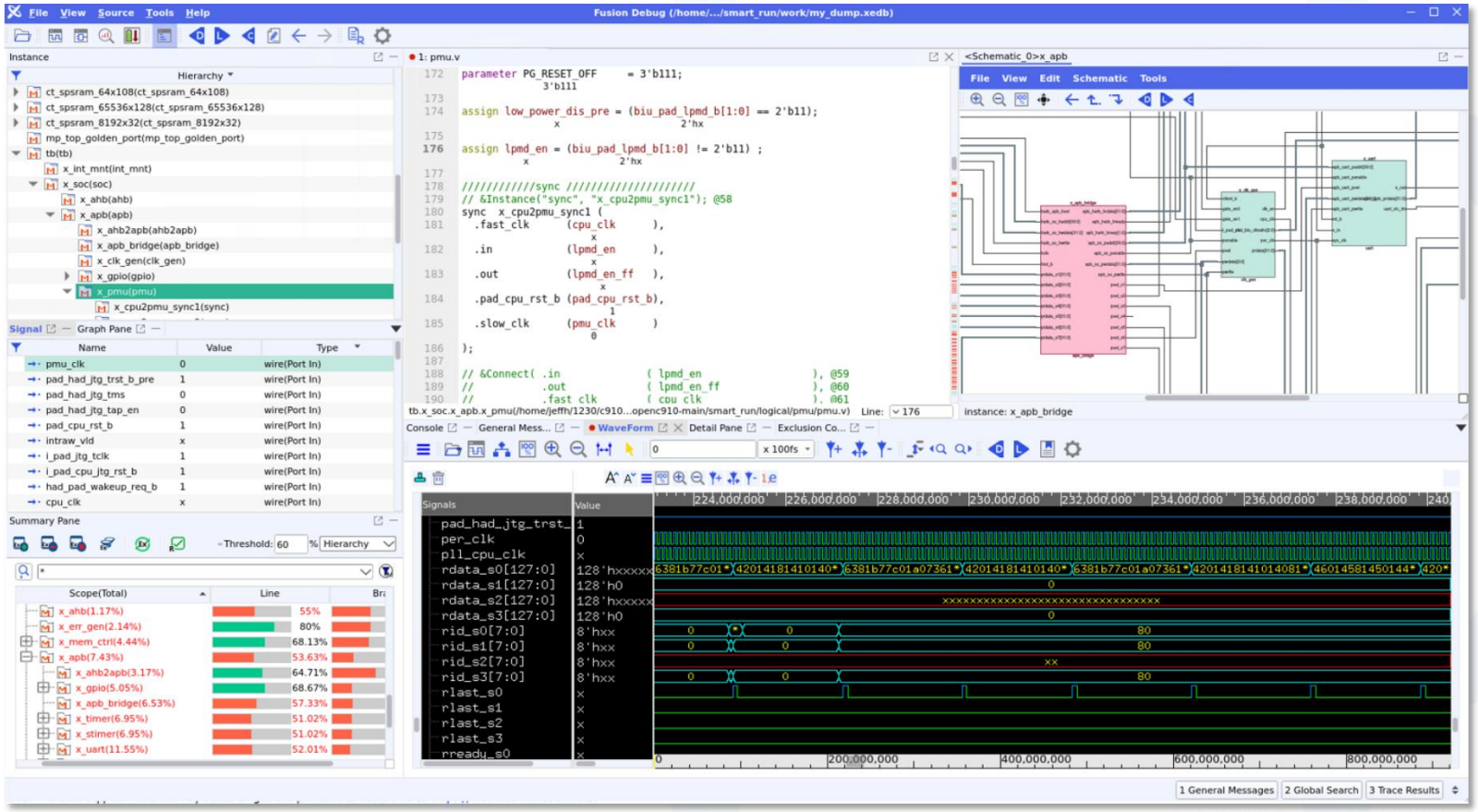


Virtual Device
MIPI / DP / HDMI / UART

Transactor base Monitor

Fusion Debug

X-EPIC



物理探针
板载 DDR 作为dump buffer
循环抓波形

流式探针
一边抓波形一边上传
边抓边看

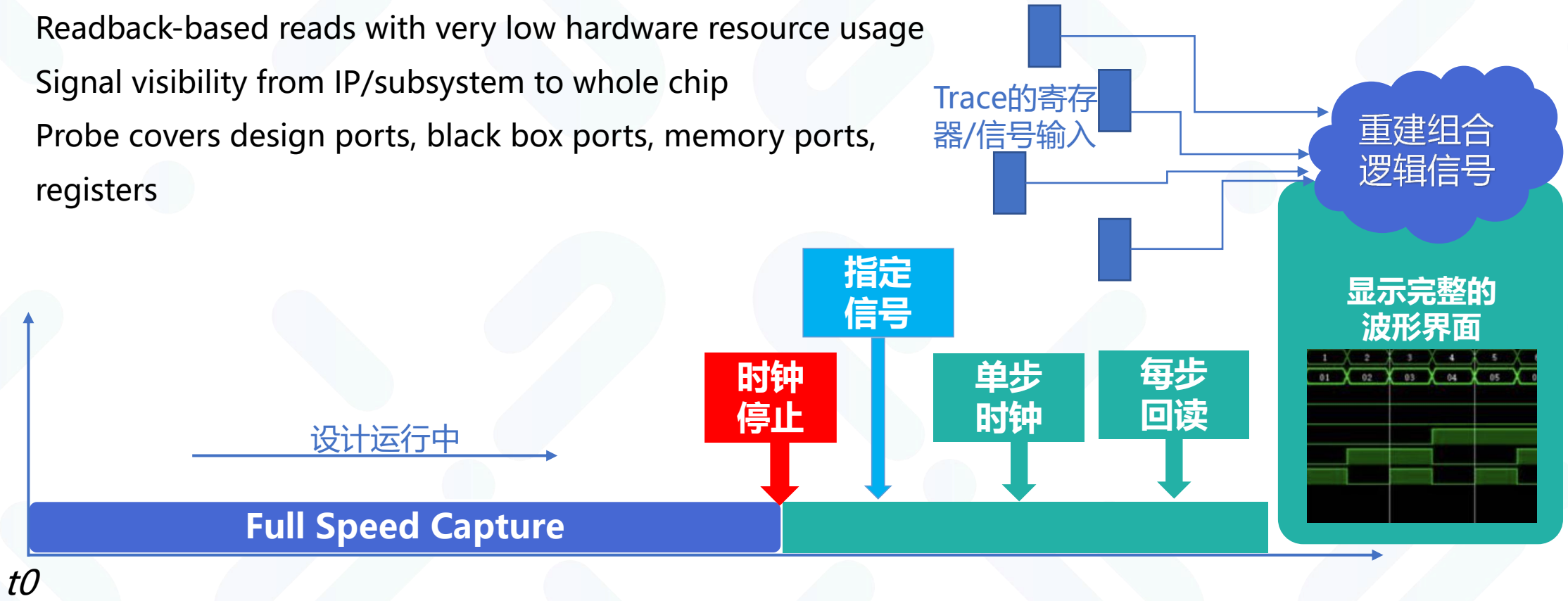
全信号波形
不限制波形的深度和位宽
抓全系统波形

运行时内存后门读写
Sram / DDR 子卡 / DFI Model

运行时信号后门读写
get, force, release, deposit

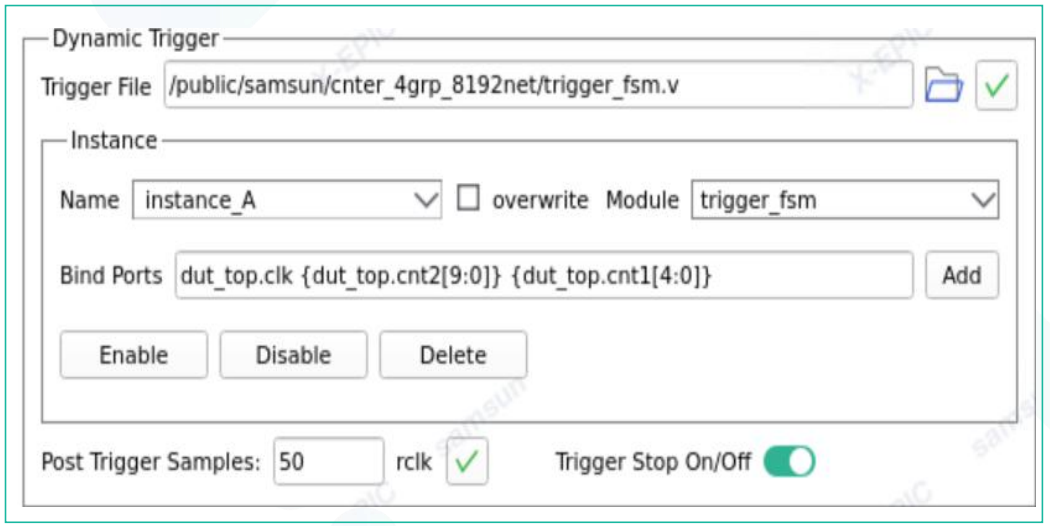
Full Vision

- Powerful parallel waveform reconstruction algorithm for high-speed waveform recovery
- No need to re-specify signals before compilation
- Readback-based reads with very low hardware resource usage
- Signal visibility from IP/subsystem to whole chip
- Probe covers design ports, black box ports, memory ports, registers



Trigger with State Machine Support

- ✓ 支持任意层次信号触发，无需重编译
- ✓ 精确触发无漂移
- ✓ Verilog语法的触发状态机建模
- ✓ 支持触发信号间更丰富的运算条件
- ✓ 支持多个状态机并行触发
- ✓ 触发后自动执行调试命令
- ✓ 保持较高运行速度



Case： Multicore CPU System

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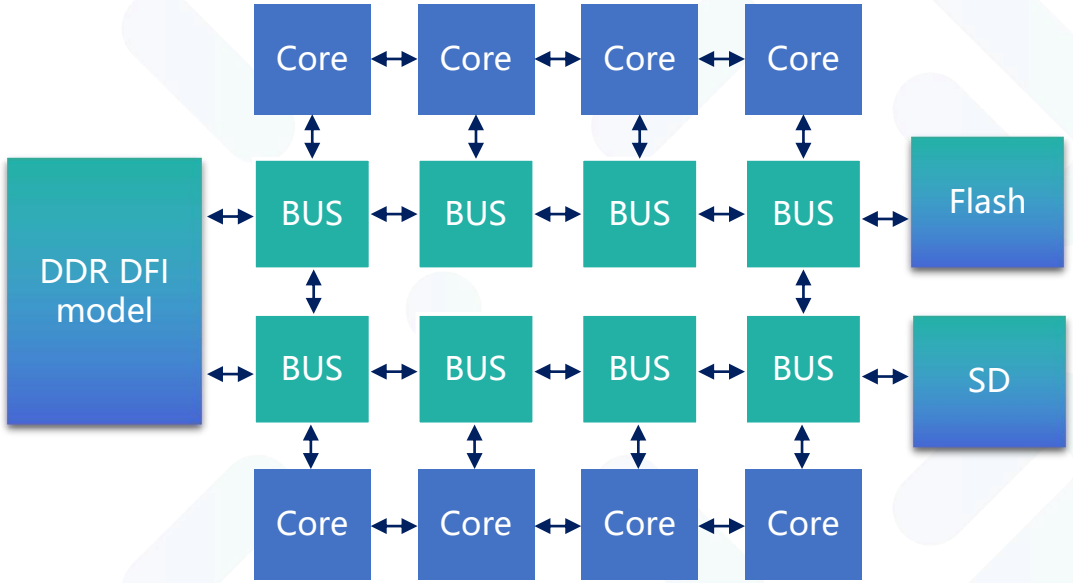
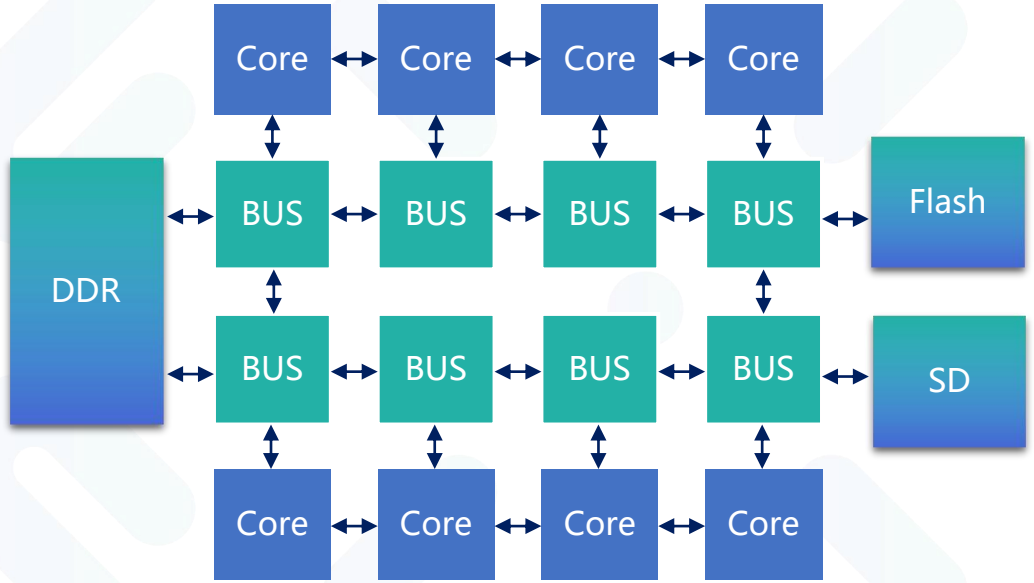
Emulation



Prototyping



CPU 2M / BUS 1M / DFI 2M

clock

CPU 50M / BUS 10M / DDR daughter card 200M

Core Function / Benchmark
BUS Performance / Pressure

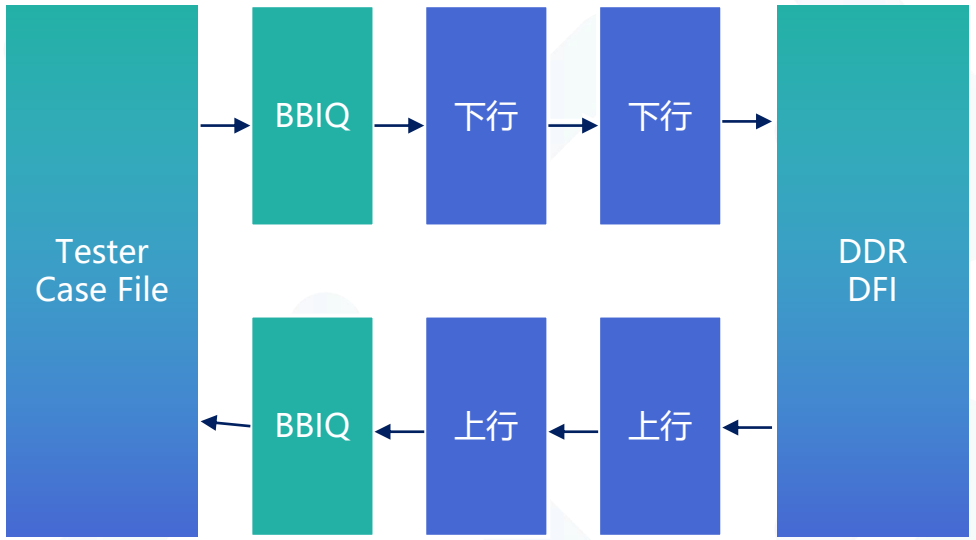
TeseCase

OS Booting
Driver Develop

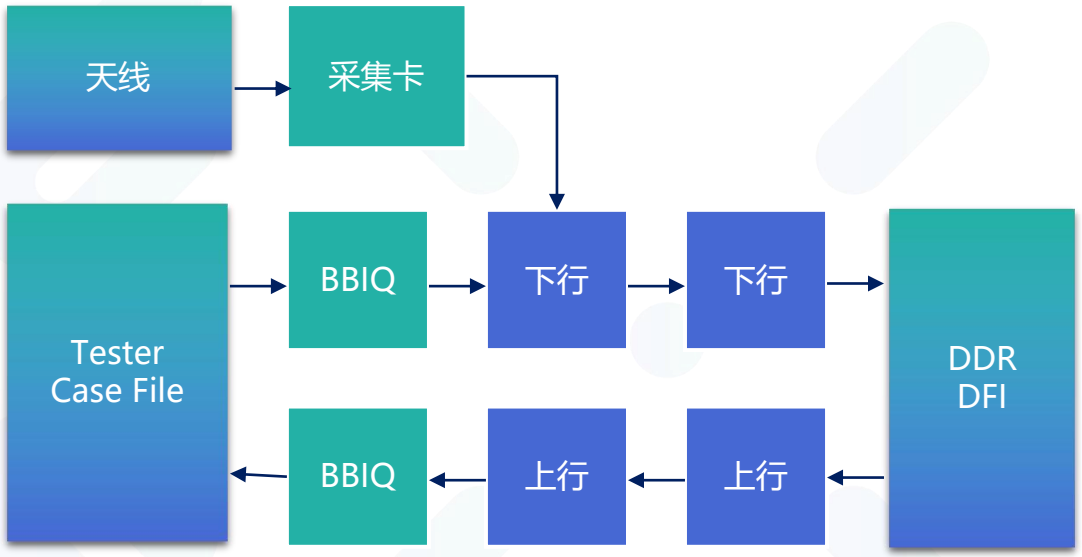
Case：5G 终端

X-EPIC

Emulation



Prototyping

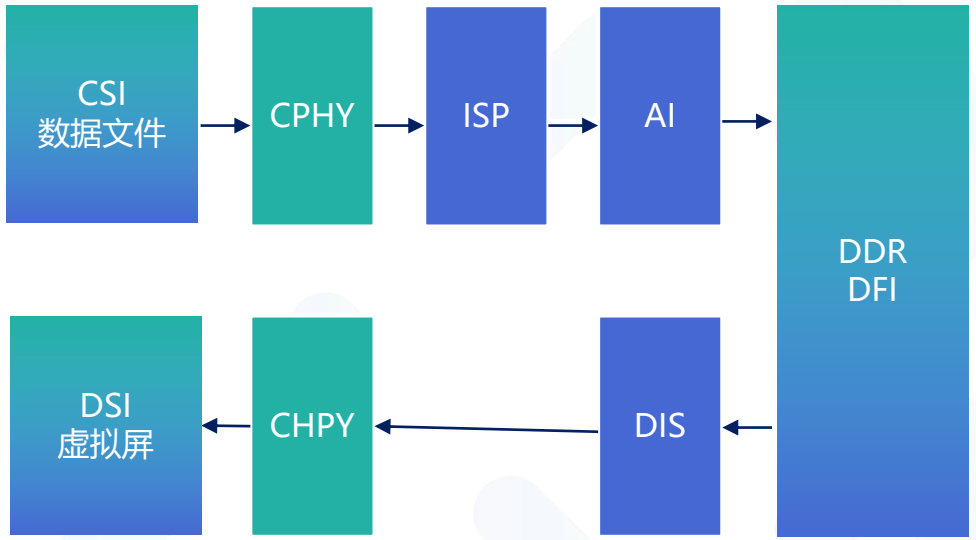


1 ~ 2M	时钟	50 ~ 100M
Function / Regression BUS Performance / Pressure	验证项目	OS Booting / 协议栈 Driver Develop

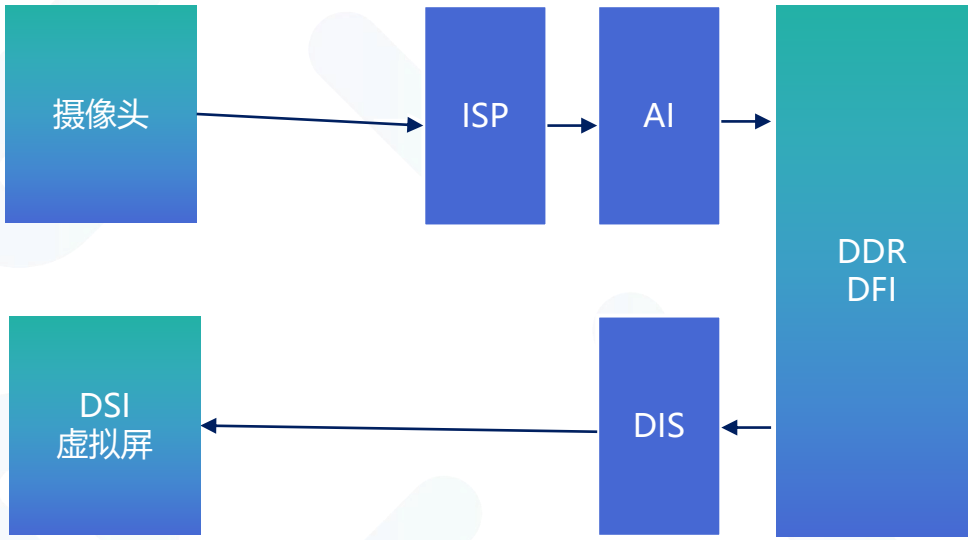
Case： 视频处理

X-EPIC

Emulation



Prototyping



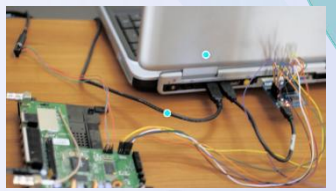
Prototyping OR/AND Emulation

X-EPIC

Prototyping

system validation

system prototyping

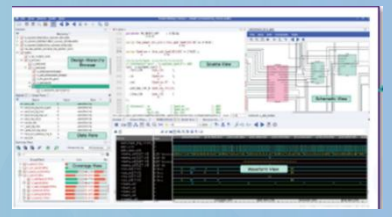


Software development

Speed Bridge

Transaction Base Acceleration

Virtual Host
Virtual Platform

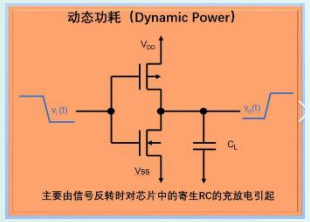


Debugging

Virtual Device

Emulation

Performance



Power Analyze

Pressure testing

X-EPIC

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