2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA

accellera SYSTEMS INITIATIVE

DESIGN AND VERIFICATION ™ CONFERENCE AND EXHIBITION

Shanghai | September 20, 2023

Escalating requirements for SoC verification using real software applications

How to optimize emulation and prototyping resources

Vijay Chobisa
Senior Director

SIEMENS

Agenda

Industry trends and growth drivers

Verification and validation challenges

Optimized Hardware-Assisted Verification (HAV) use

Summary

Q&A

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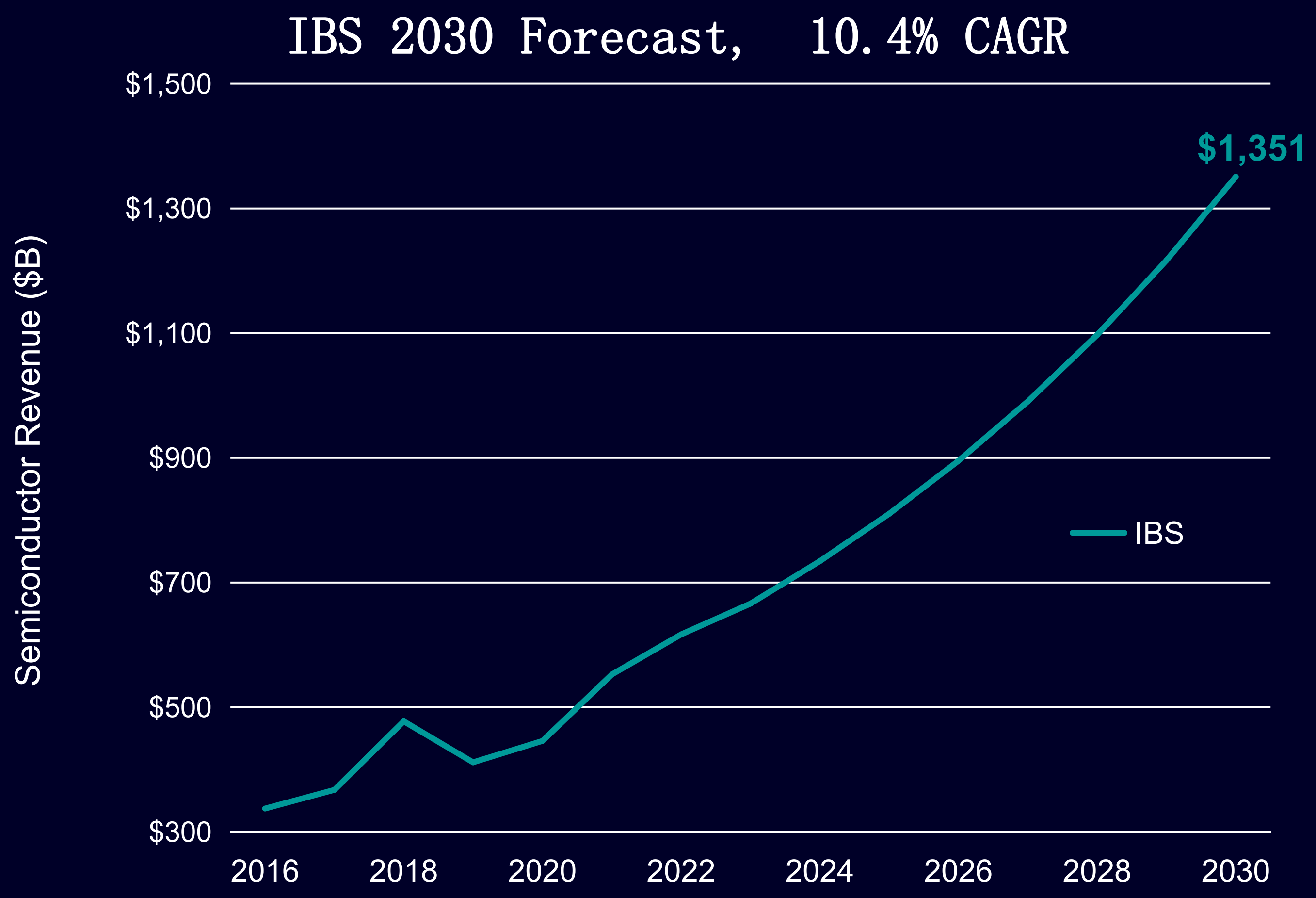
Industry trends and growth drivers

Semiconductors and electronics innovation are the drivers of digitalization; the rapid deployment of AI, cloud, 5G, and edge computing will fuel spectacular growth



Semiconductor potentially a **$1 trillion market** by 2030

Source: International Business Strategies (IBS), January 2022
VLSI Research, March 2022

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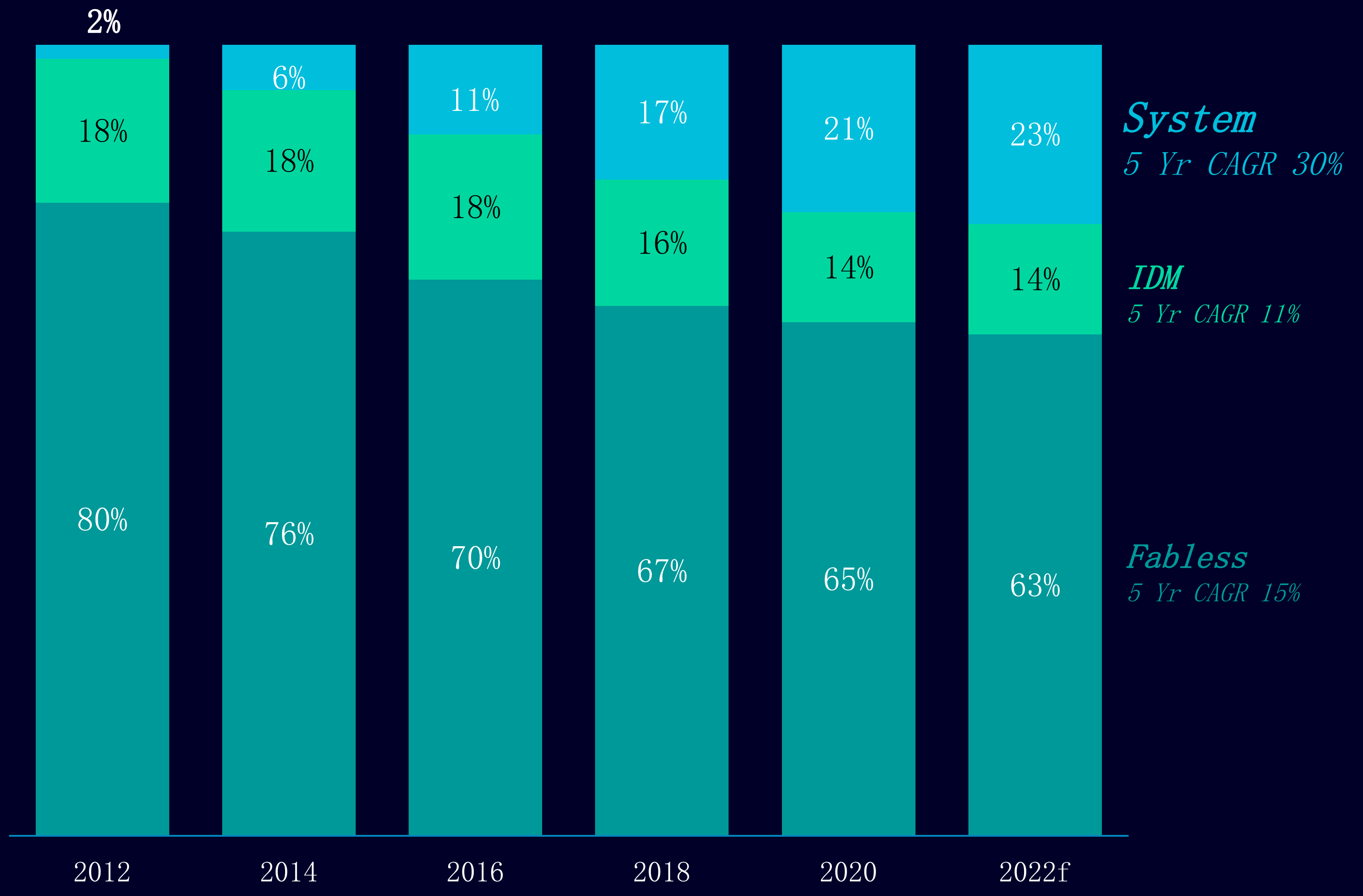
Leading-edge systems companies are becoming the new System-on-Chip designers

Share of Pure-Play Foundry Revenue (%)



Source: Siemens EDA Analysis and IC Insights McClean Report, November Update 2022

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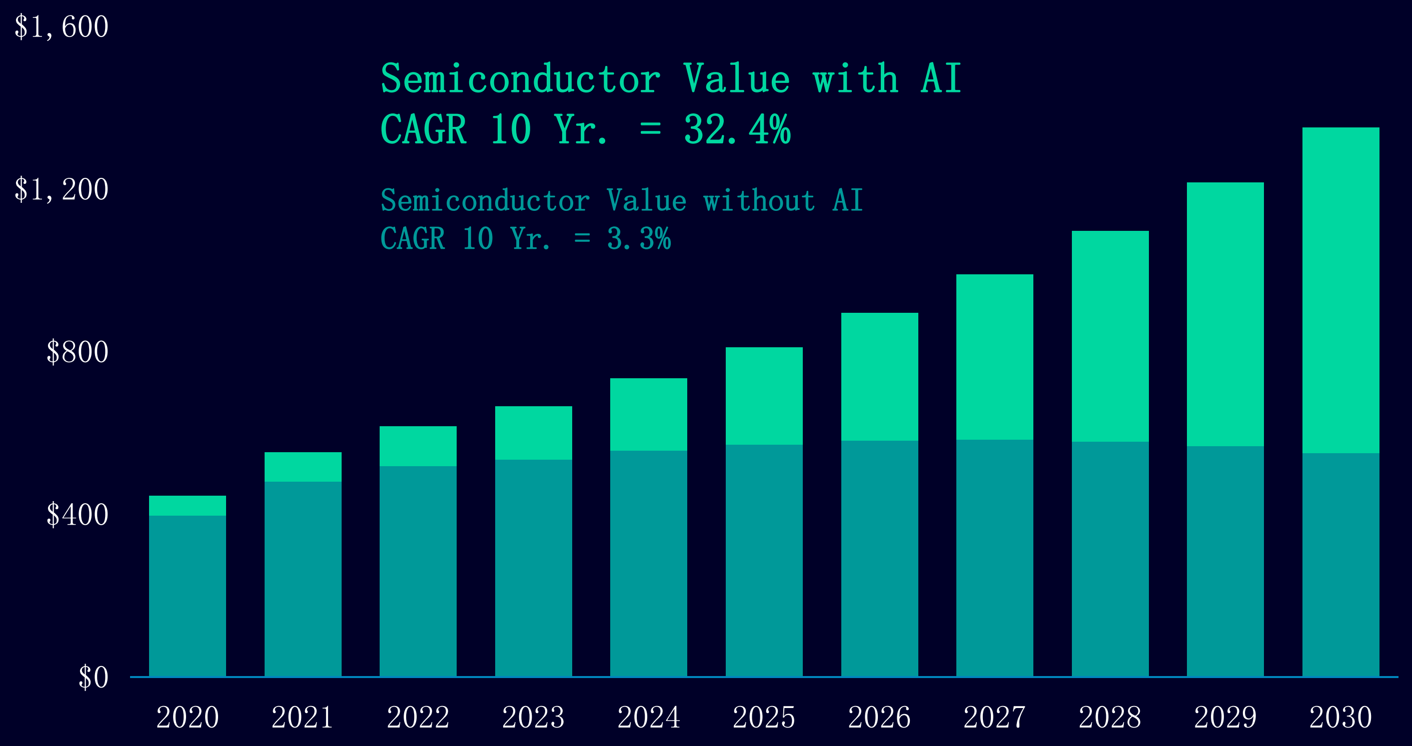
Unique AI content is a major semiconductor driver



Source: IBS May 2022

AI Hardware is the leading driver of semiconductor content and silicon usage

General purpose IP is insufficient when power and performance are key to the application success

Adaptability to create unique silicon content rapidly will drive the next generation of applications

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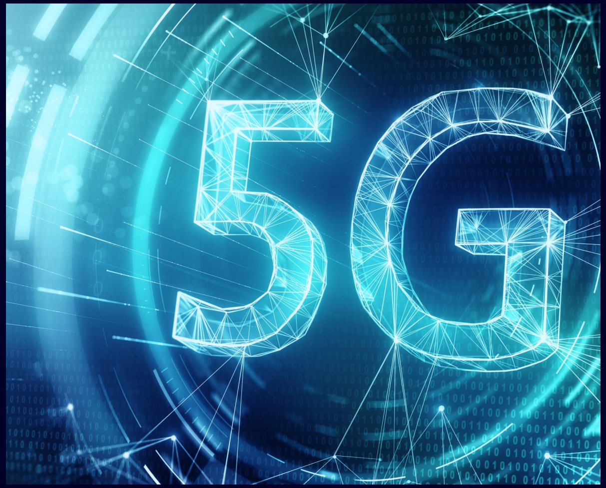
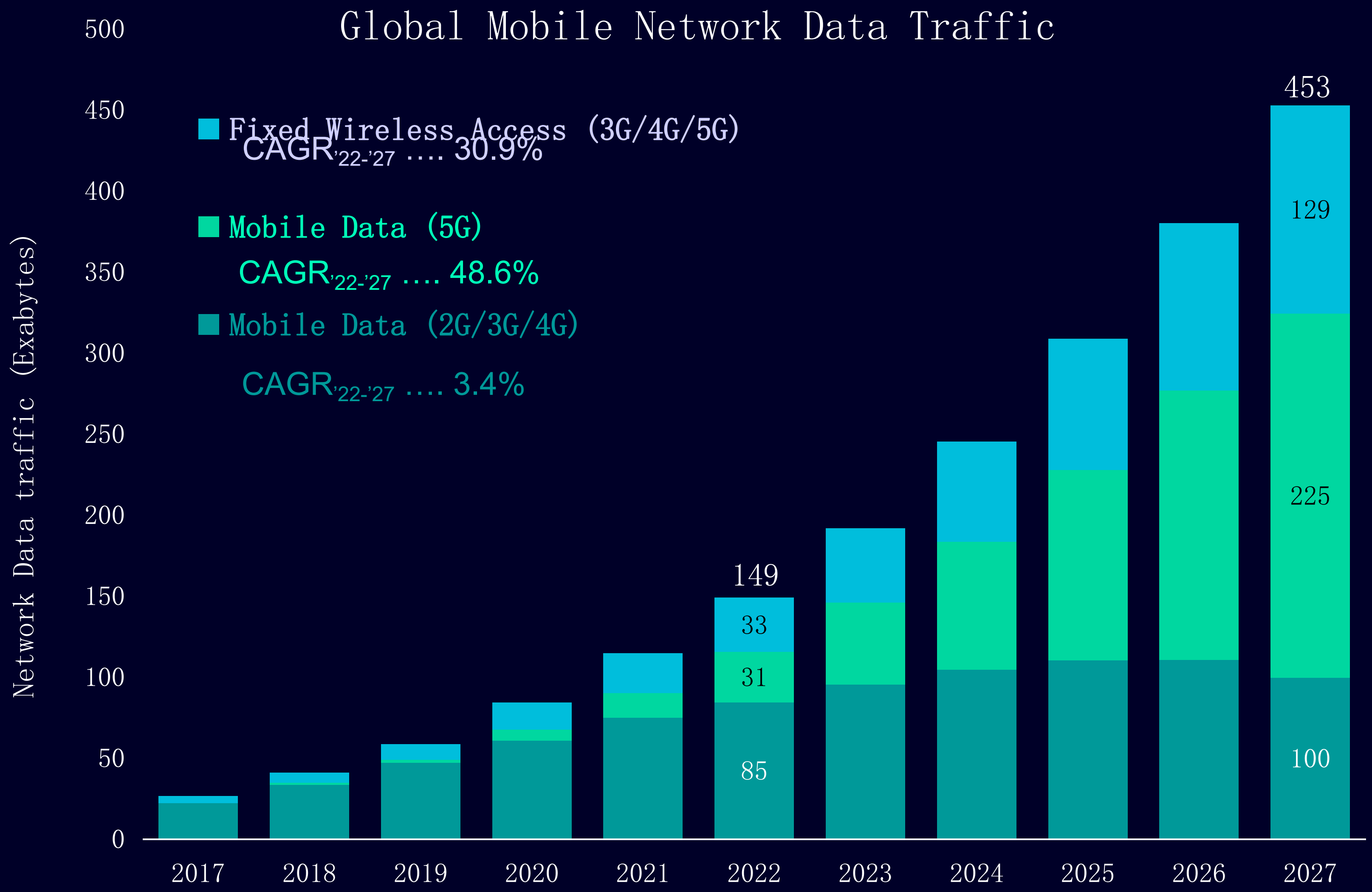
Global mobile Network traffic reached 149 Exabytes in 2022 growing to 453 in 2027



In 2022 – 5G smartphones consumed ~40% more semiconductors than 4G smartphones on average



Source: Ericsson Mobility Report, Jan 2023

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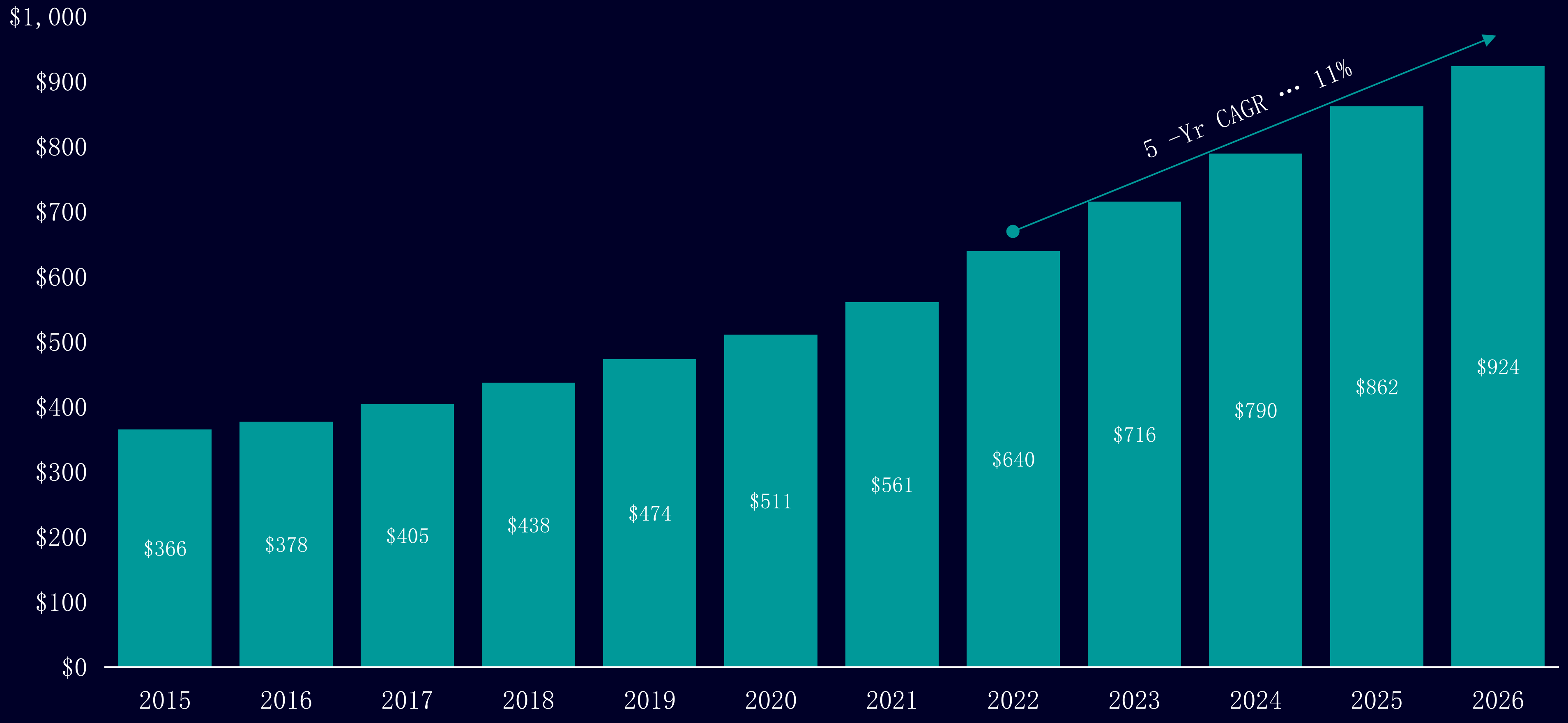
Automotive semiconductor content expected to reach $1,000 per vehicle in 2026

Automotive Semiconductor Content
Per Vehicle ($ Dollars)



Source: Strategy Analytics, October 2022 & McKinsey & Company

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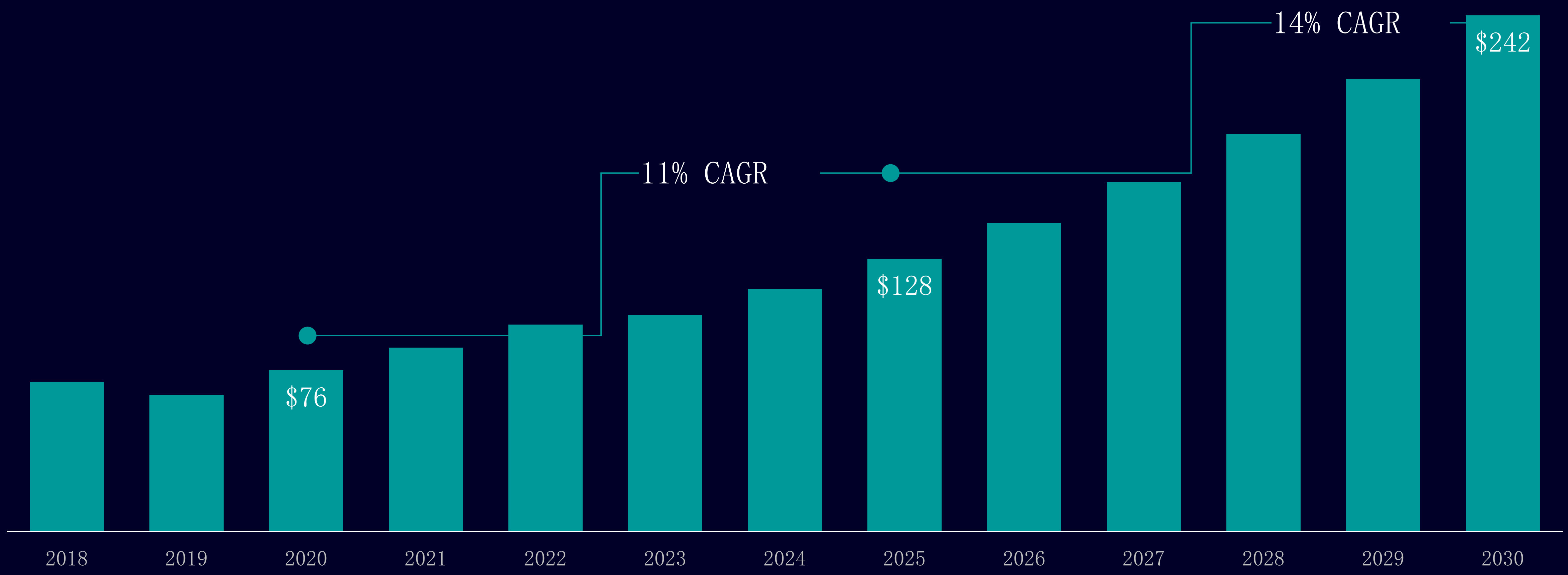
Data centers represent a high-growth opportunity for semiconductor suppliers

Semiconductor consumption in data centers ($B)



Source: IBS, Sept 2021

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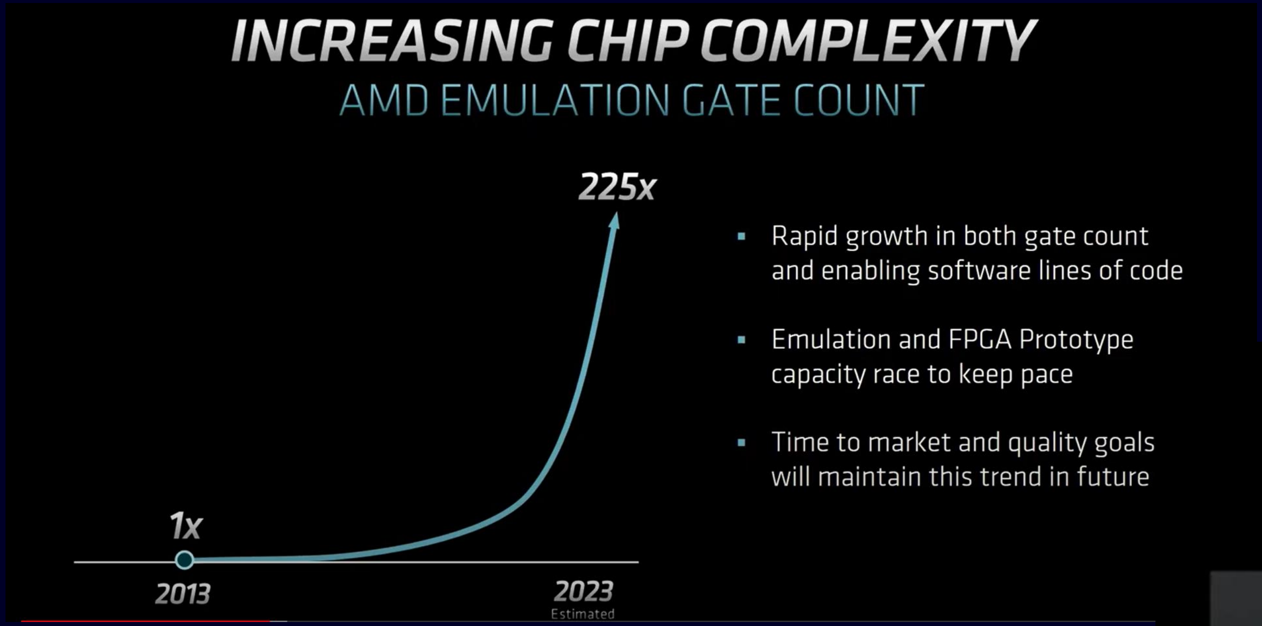
Verification and validation challenges

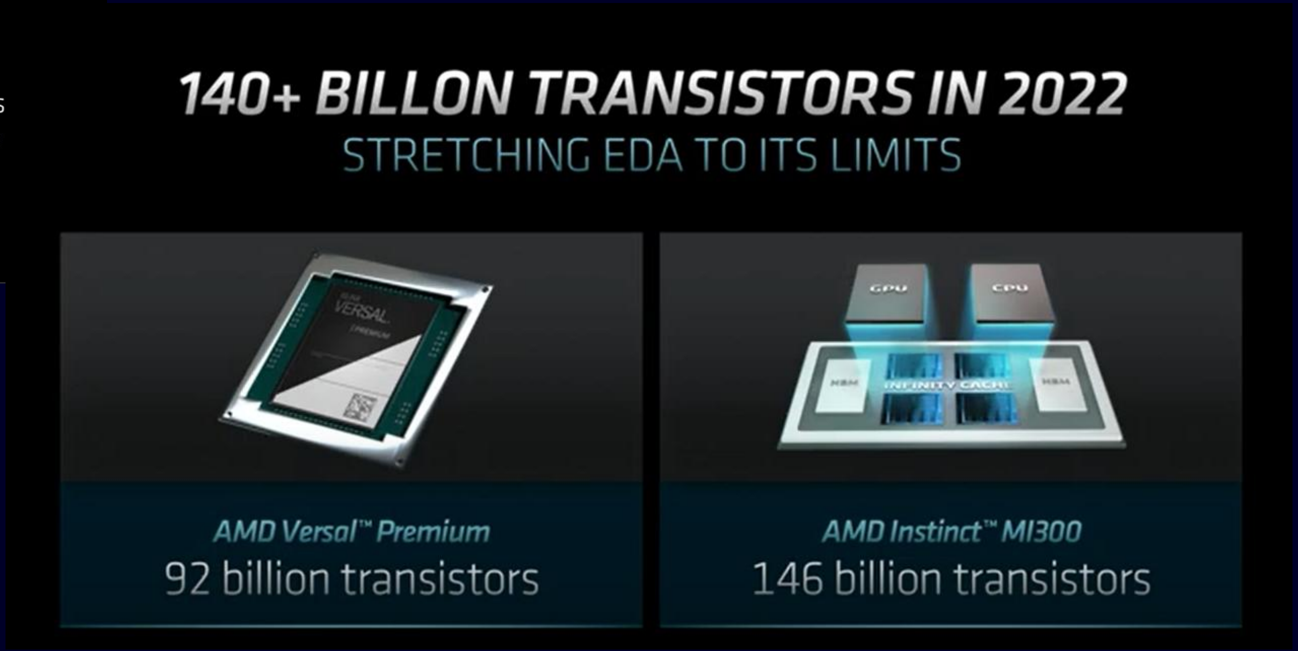
System context is increasingly critical to product success

Tuning and optimization of system software/workloads on the SoC is critical for successful design, verification and power/performance analysis

SoC functionality needs to be integrated and validated within the system context to ensure correct operation of complex systems

Mark Papermaster, AMD – DAC 2022, keynote
Advancing EDA through the power of AI and high-performance computing





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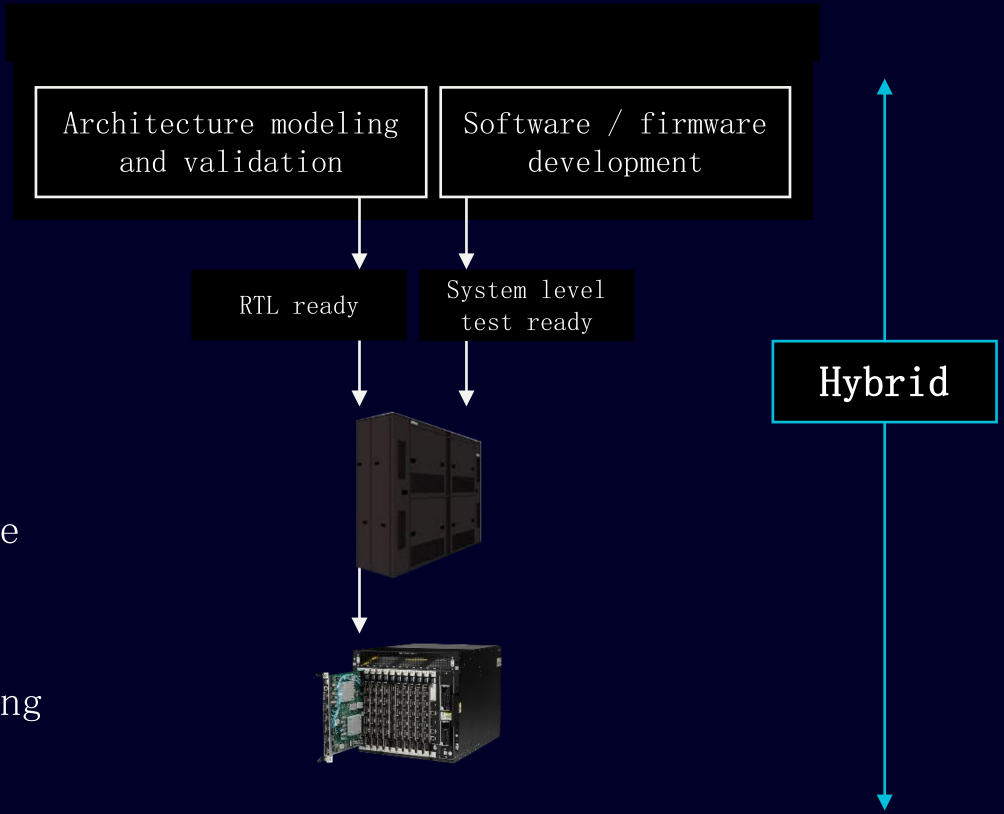
Earlier tools and infrastructure for system-level test and development

System modeling:
- System and chip architecture
- Pre-RTL software/ firmware

Big box emulators:
- Full system level testing
- Full debug capabilities
- Quick emulation model build time

Enterprise FPGA emulators:
- Higher performance system testing
- Cost effective for high volume



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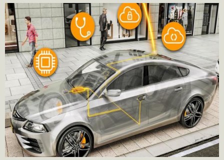
Hybrid:
- Emulation and system model
- Optimizes dev time, capacity and speed

Need seamless infrastructure of emulation and system modeling

Software defines the product in all industries

Automotive



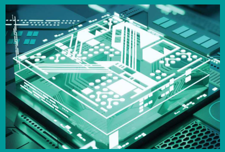
Digital Video

Mil Aero

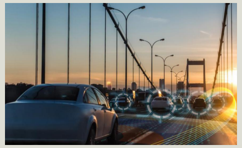
Storage

AI/ML

CPU/GPU



Networking



5G

Mobile

Complexity is derived from the software required to test the hardware and the number of customer workloads to achieve full visibility

Power & performance demands increase the complexity for HW and SW integration

Requires billions of simulation cycles and thousands of emulation cycles

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Optimized HAV use

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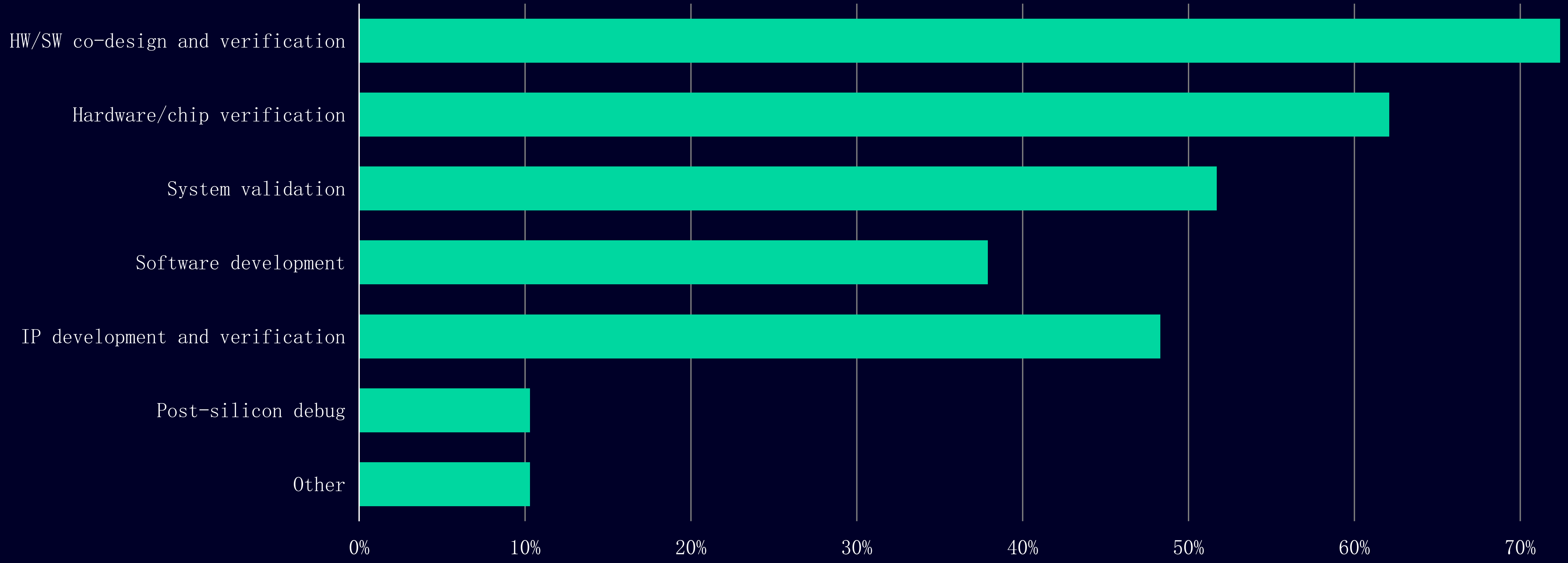
Projects use primary types of HAV technologies – emulation and FPGA prototyping



Source: Wilson Research Group and Siemens EDA, 2022 Functional Verification Study

Veloce can deliver customer value with our strong HAV ecosystem

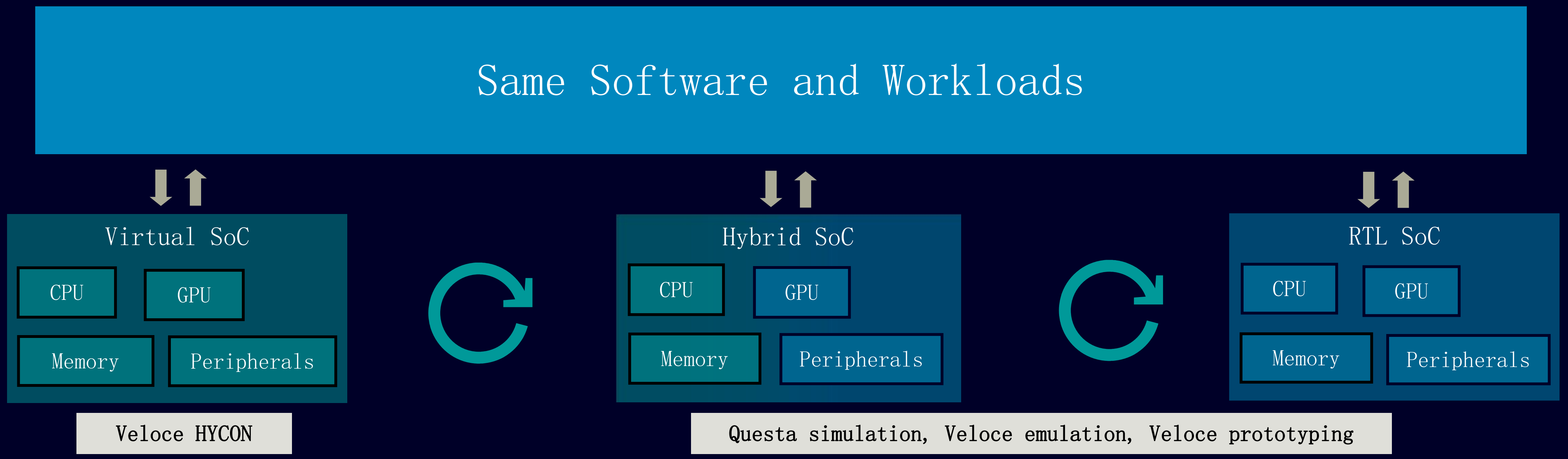
Veloce Strengths

Reliable & power efficient
Virtualization
Capacity Scaling
Broad Apps and Solutions

Customer Value

Low TCO
High Productivity
System level verification
Meet verification goals

Shift left becomes possible with a unified environment for collaboration between HW and SW teams



Leverage the platform capabilities to meet the key requirements of speed, accuracy and debug

HAV apps are critical for full system-level verification

Power analysis + UPF
System level power analysis on real software workloads

HW/SW co-verification
Debug HW-SW integration issues with advanced tools

Coverage and assertions
Leverage metric-driven verification for coverage closure and effective debug

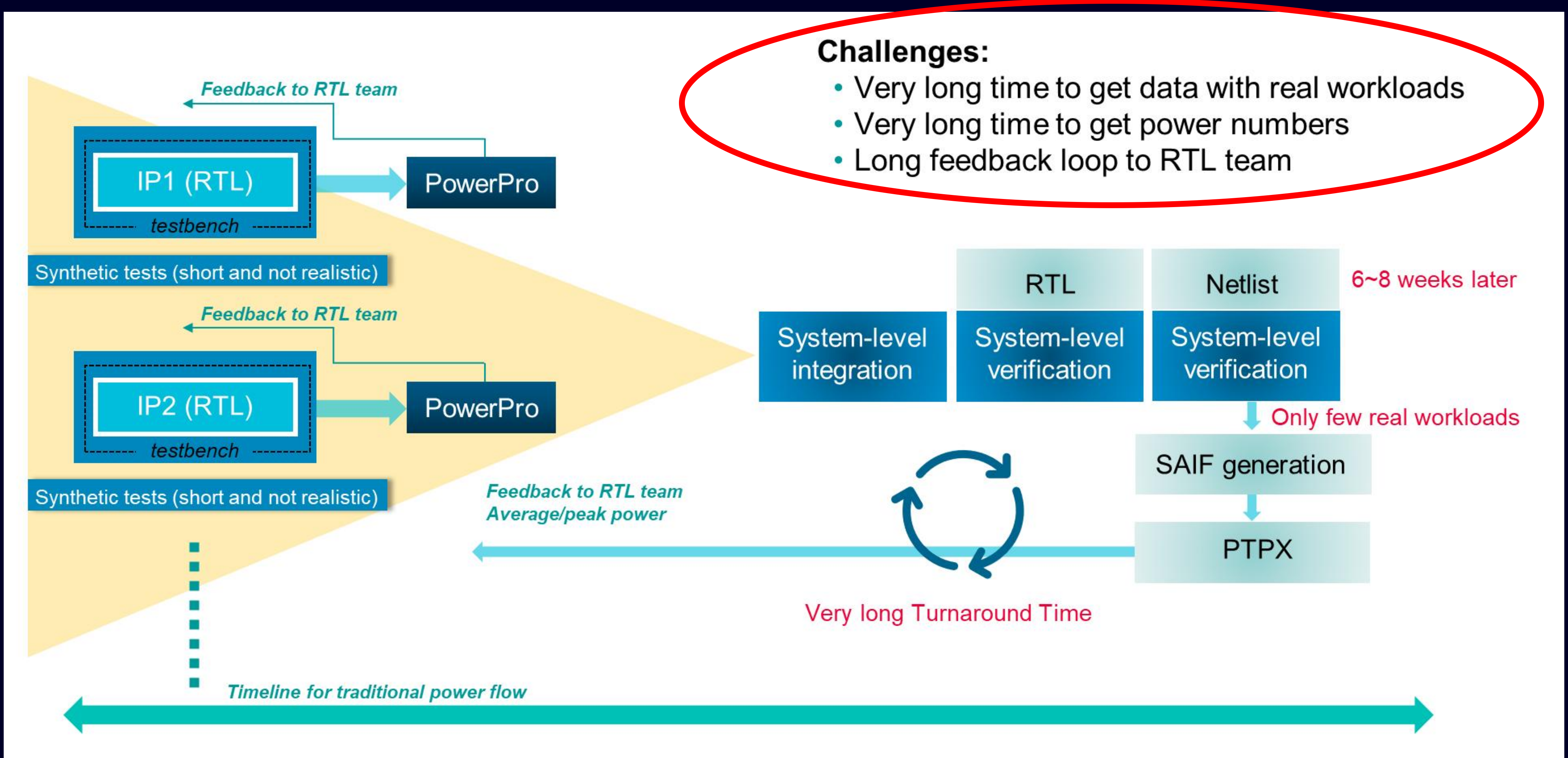
Apps to meet all verification challenges

Software validation
Validate full SW stack across virtual, hybrid and HW designs

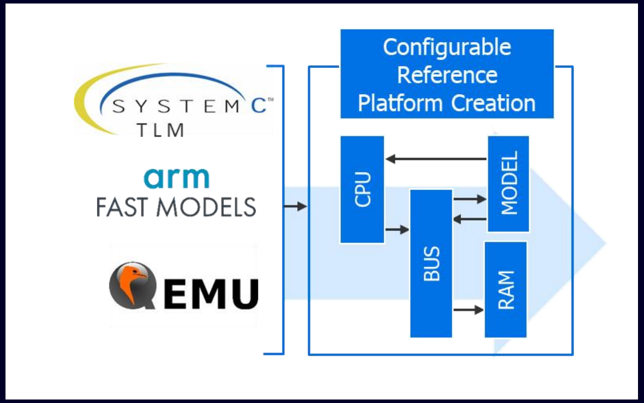
DFT and fault
Validate test patterns, functional safety and ISO26262 certification

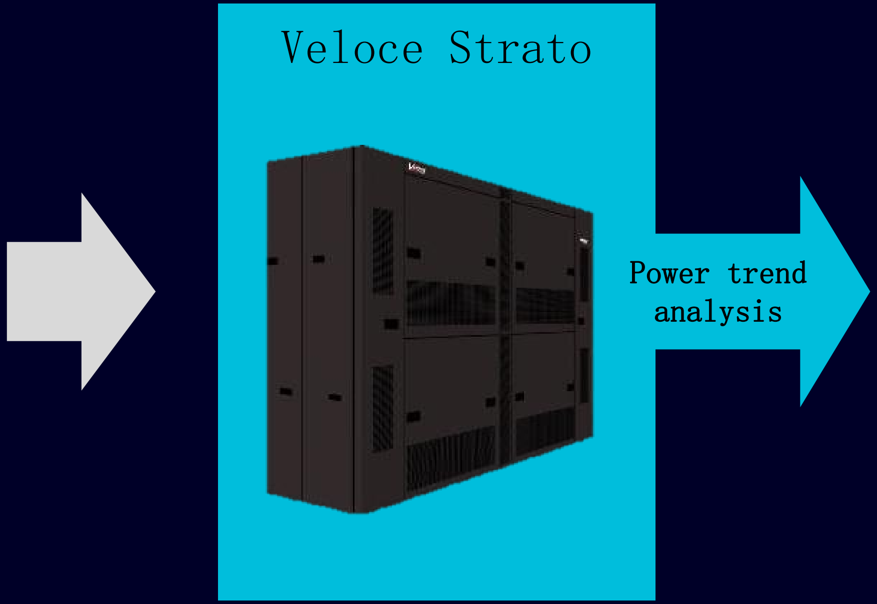
Enterprise server
Manage emulation resources and optimize job placement

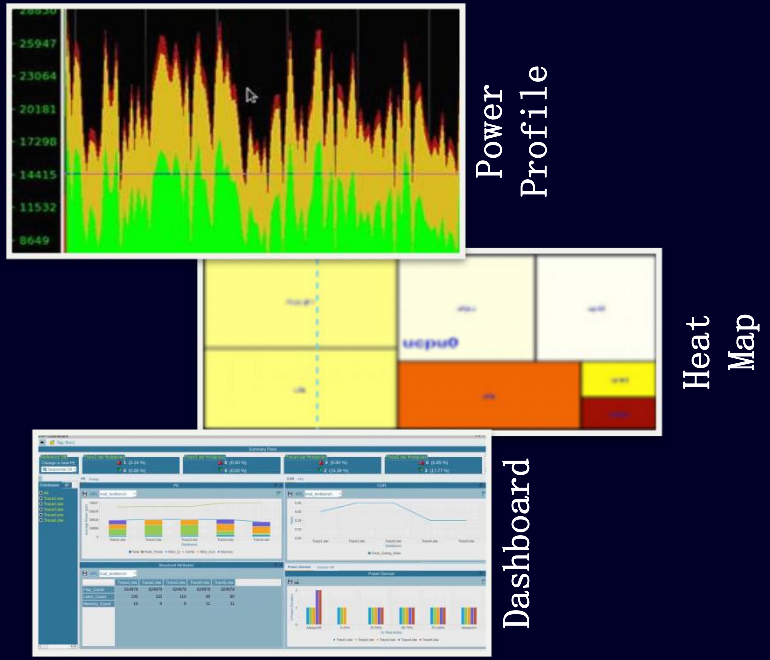
Traditional power flow



Shift left power analysis done at the system level







Customer design	Design size (MG)	Design cycles (M)	Emulation exec time	Plot generation
Display core	130	40.7	0:13:42	0:16:23
CPU	**450**	**550**	**0:45:18**	**1:00:14**

Generating power profile for 100s of millions cycles

Enable decisions based on real-world data

Scenario not possible to simulate without hardware acceleration

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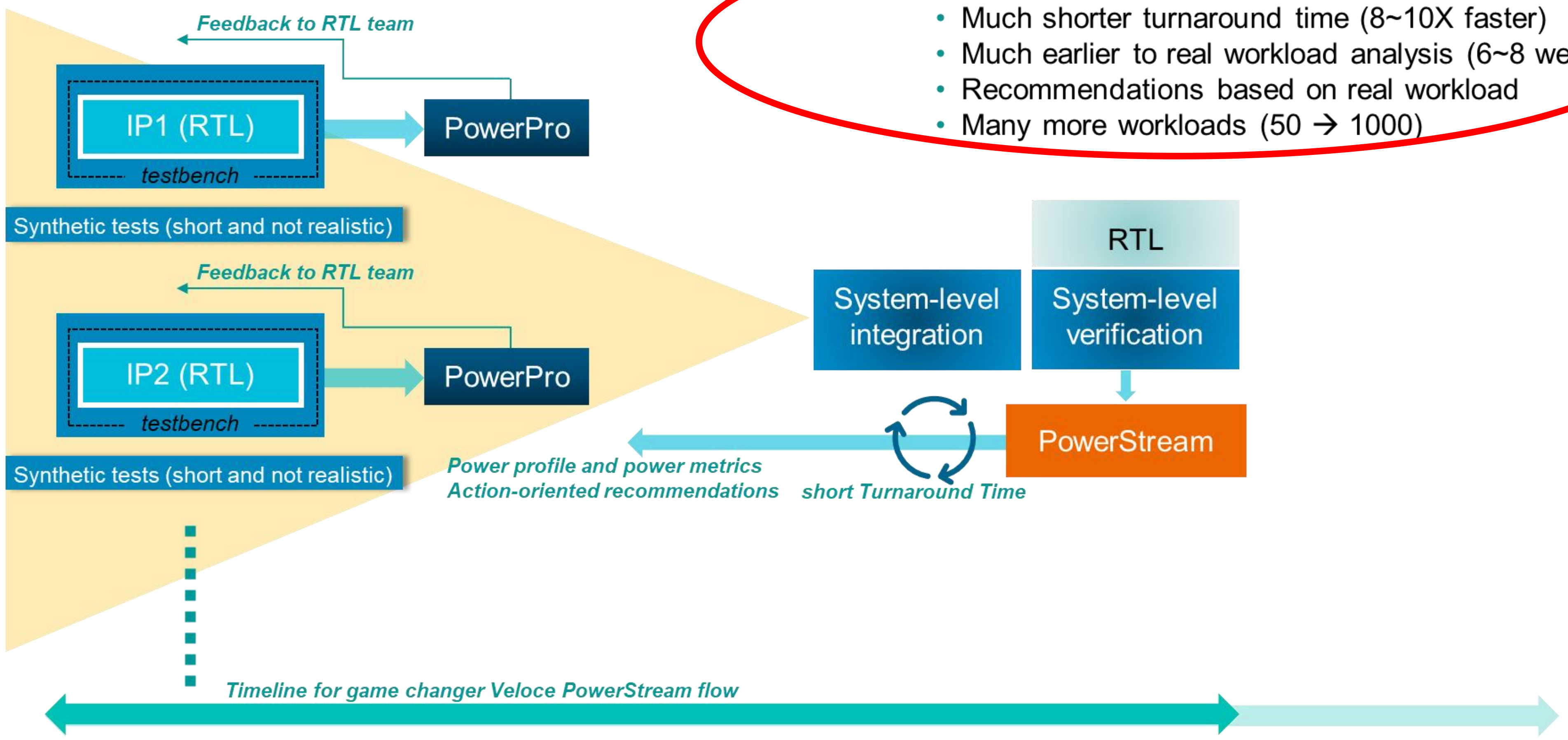
Veloce PowerStream is a game changer

arm User2User

Benefits:

- Much shorter turnaround time (8~10X faster)
- Much earlier to real workload analysis (6~8 weeks)
- Recommendations based on real workload
- Many more workloads (50 → 1000)



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Autonomous vehicle design and verification methodology platform

- Evaluate multiple levels of abstraction for models of systems and SoCs
- Understand performance from the silicon to the complete system including driving scenarios
- Run entire software stacks, providing metrics of power and performance

Veloce System Interconnect

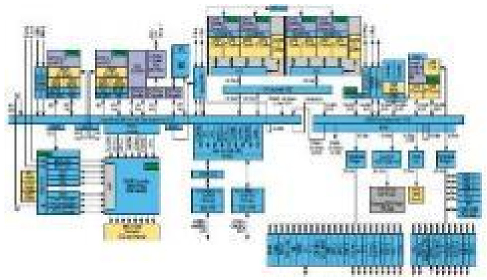
Open Interface Layer

FMI FUNCTIONAL MOCK-UP INTERFACE + TLM + DPI

Sense

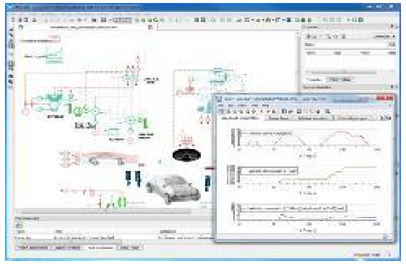
Decide

Virtual & RTL Design



Veloce Hardware Accelerated Verification

Actuate



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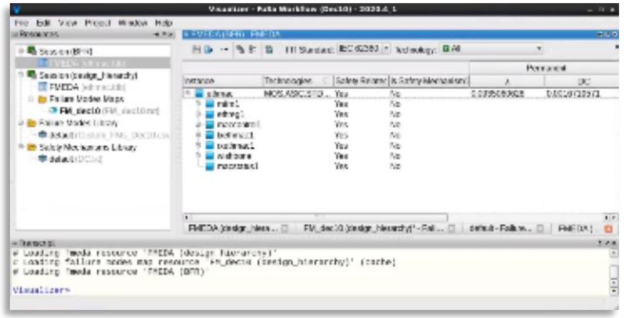
Safety critical automotive IC development introduces new challenges

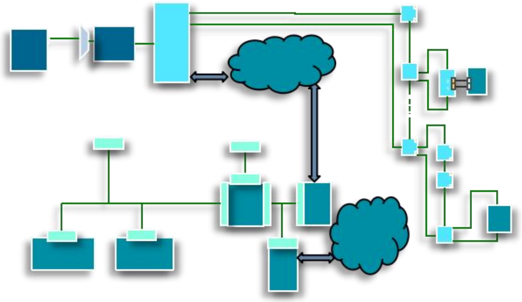
ISO 26262

Safety Analysis



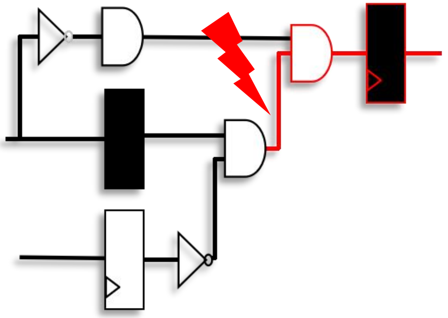
Early safety analysis that provides a path to an **optimal safety architecture**

Safety Insertion



Efficient, consistent, and **insertion** of safety mechanisms to achieve the safety architecture

Safety Verification



Multi-domain **fault injection to** prove the effectiveness of safety architecture

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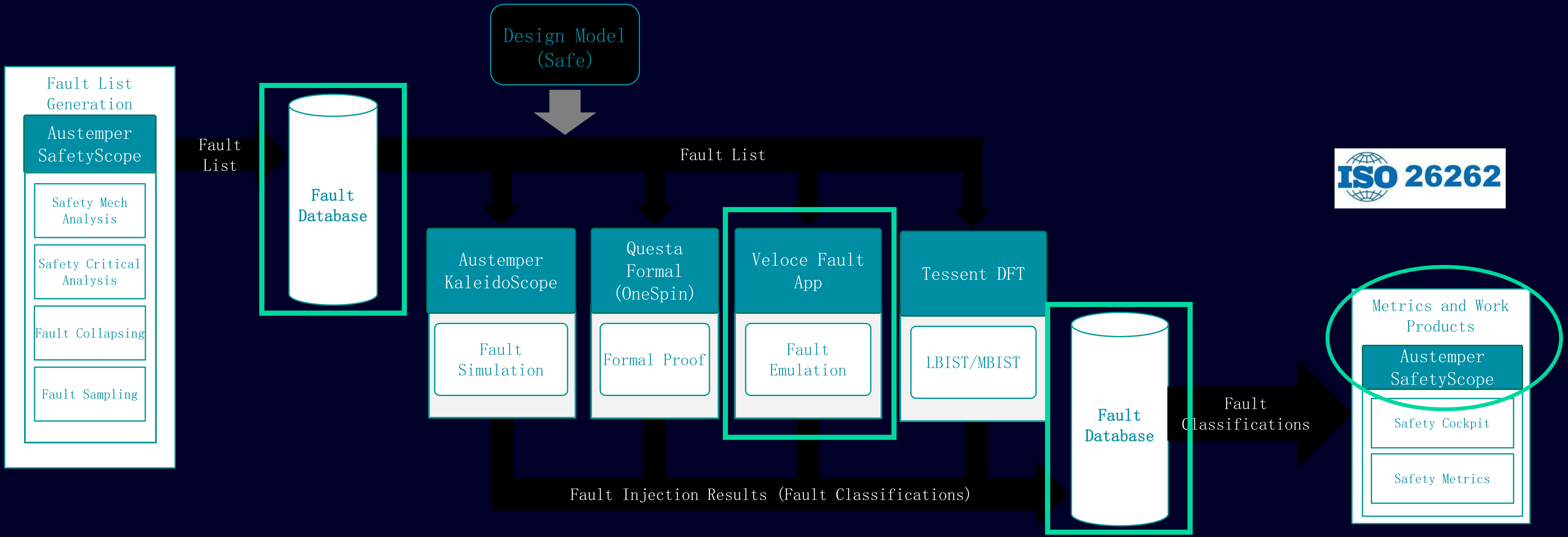
Siemens EDA integrated fault injection solution



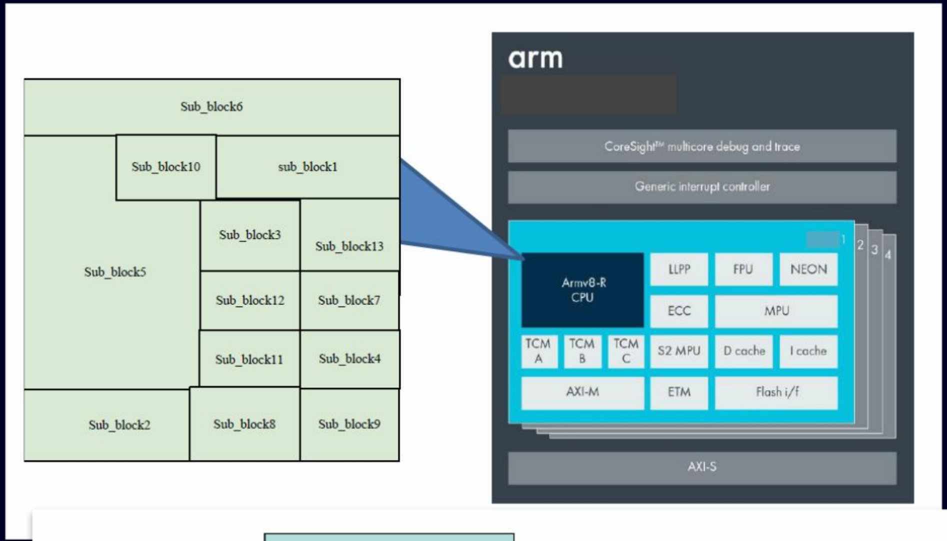
Generate an **optimized fault list.**

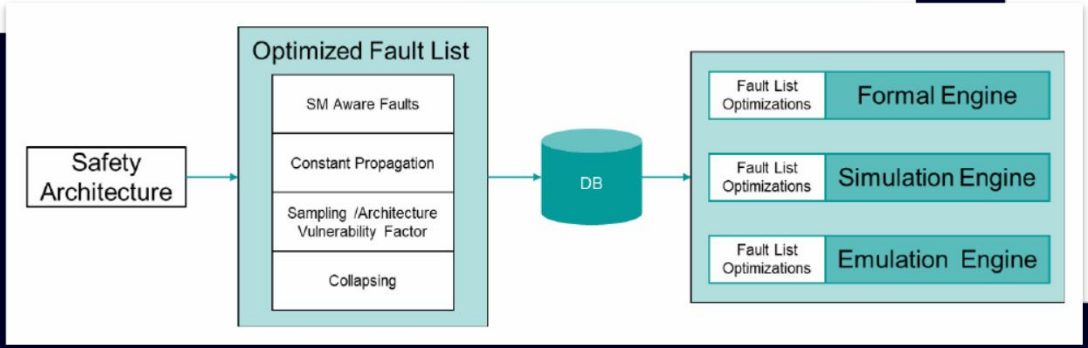
Fault Injection engines **read fault list, execute fault injection,** and **classify faults**

Generate **safety metrics** and **work products**

Functional Safety: Samsung Case Study

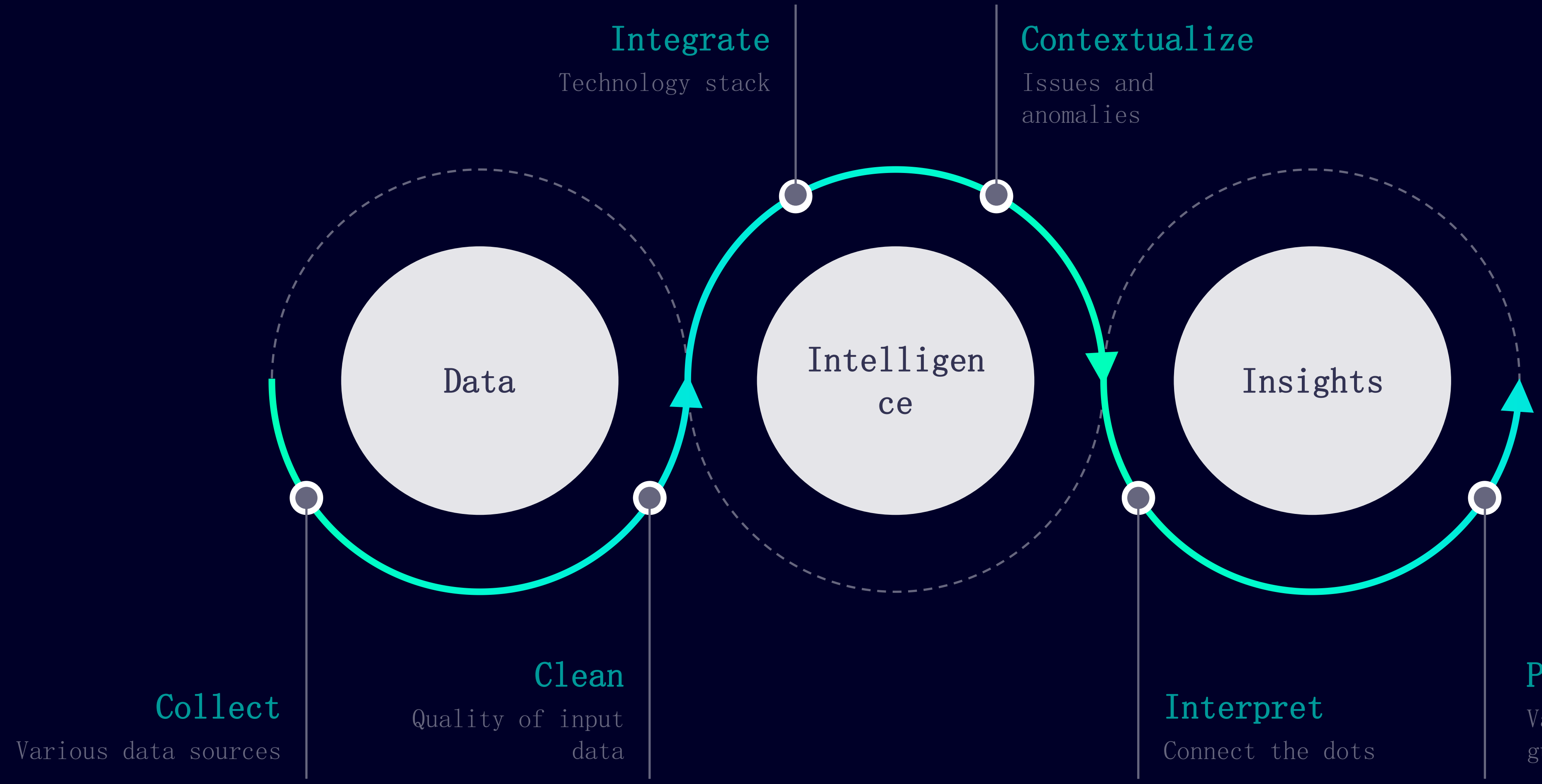
Complex Safety Mechanisms Require Interoperability and Automation For Validation And Metric Closure





Final Result	Total Faults (SA0 + SA1)	Total Fault Distribution (%)
Detected Observed	3125	77.18
Detected Unobserved	0	0.00
Undetected Observed (Residual) 10 fault moved to SAFE Fault	69	1.70
Undetected Unobserved (conservatively Residual)	280	6.92
Safe Fault Dead Logic	234	5.78
Safe Fault Formal COI analysis Signal Back Propagation Safe Fault Configuration Engineer's justification	341	8.42
sub total 4782 – 733 (Not Injected)	4049	100.00

Leverage workload data and system-level context to drive actionable insights



HW and SW instrumentation to capture data for analysis and visualization

Improve overall design and workload efficiency

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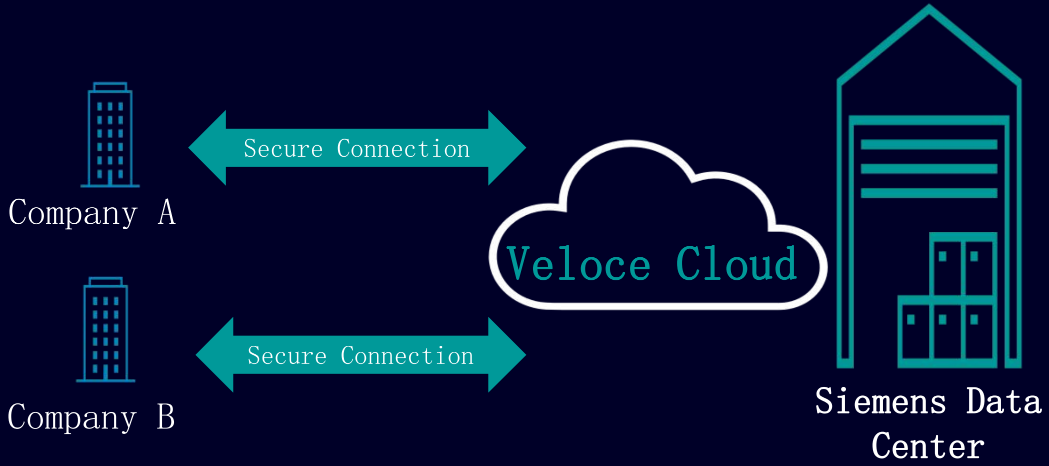
Veloce Cloud delivers secure and dynamic peak or sustained capacity



Flexible multi-tenant and multi-user solution

Secure VPN connection provides logical extension of the customer network

Veloce Cloud Emulation-as-a-Service

- delivering turnkey solutions for HW assisted verification
- services range from cloud-based collaboration to best-practice execution and emulation flows

Veloce Cloud Infrastructure-as-a-Service

- emulation expertise in house
- sustained incremental or peak capacity needs

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Summary

System-level context is essential for delivering power and performance results to post-silicon goals.

Amber Nilabh, Senior Director & GM,
Product Enabling Solutions Group
Intel

Chip size, complexity, chiplets are making verification of systems challenging and driving the need for new methodologies.

Mark Papermaster, CTO
AMD

There is a need for system modeling with abstract models for architecture exploration.

Bill Reaves, VP central engineering
Marvell

General purpose ASICs are falling short for power and performance requirements. New customizable and adaptable chips are the future for semiconductors.

For every market segment: automotive, Mil aero, storage, AI and ML, mobile networking and HPC, software is defining the hardware architecture.

The Veloce team has a history of defining the future by collaborating with customers.

By leveraging customer know how we have created the world’s most advanced HW-assisted platform.

This is what defines the Veloce Team

Q&A

Contact

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