2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA

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DESIGN AND VERIFICATION™ CONFERENCE AND EXHIBITION

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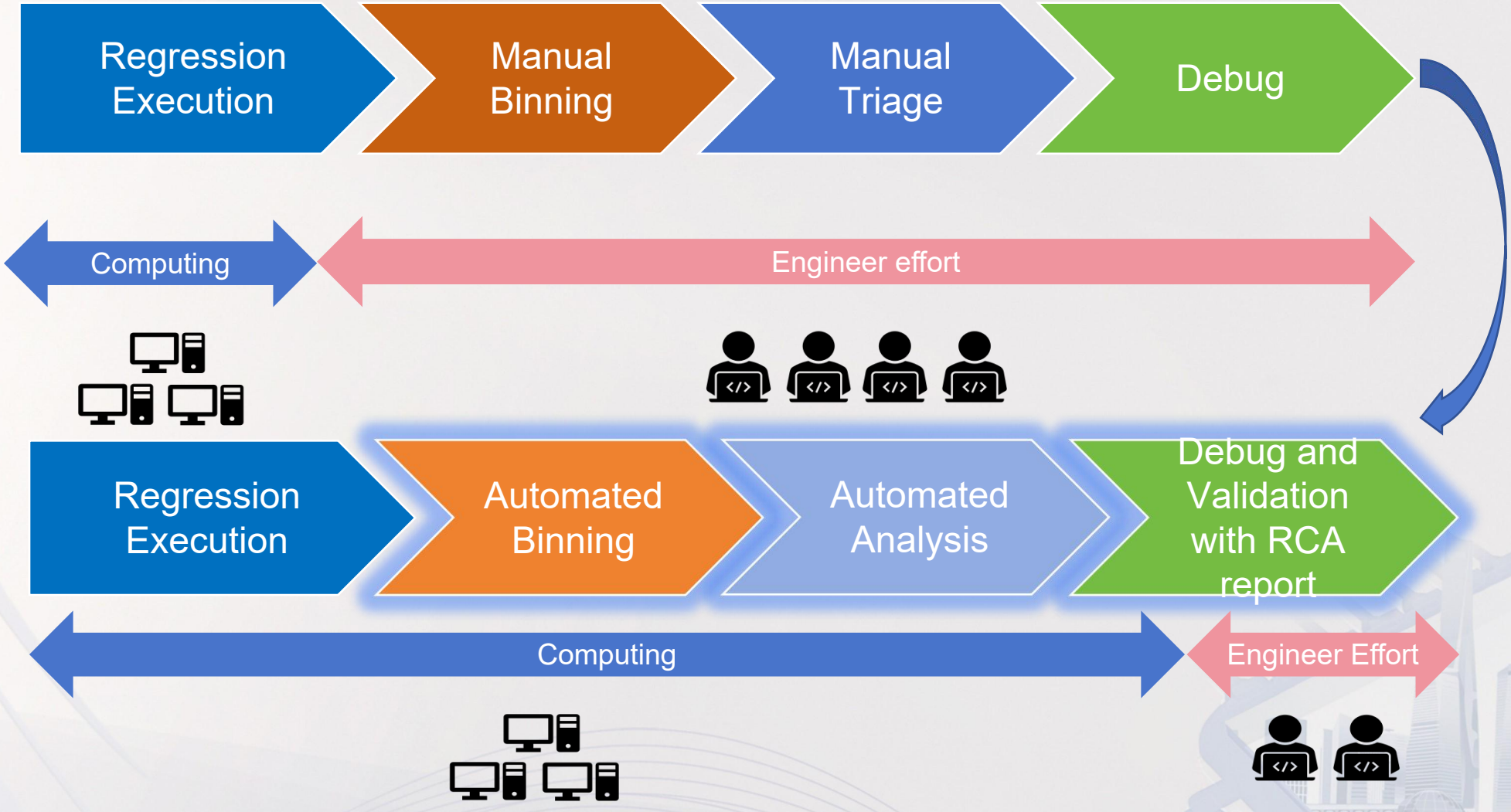
Debug Automation with AI

Yuesen Lu, Jinnan Huang
Verdi R&D, Synopsys Shanghai

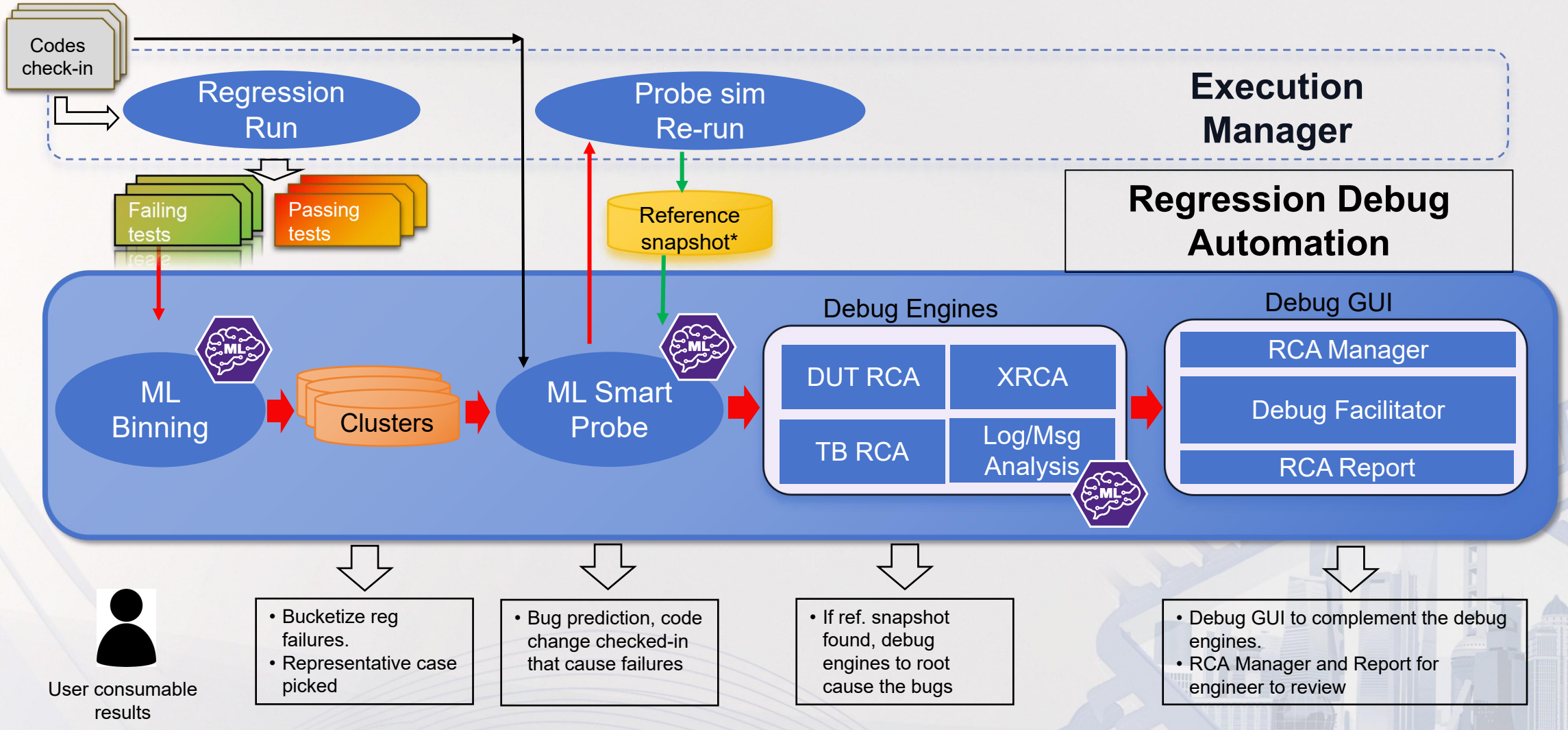
Motivation and Debug Flow

Regression Debug Automation Motivation



Reduce engineering effort and TAT with ML and advanced RCA technologies

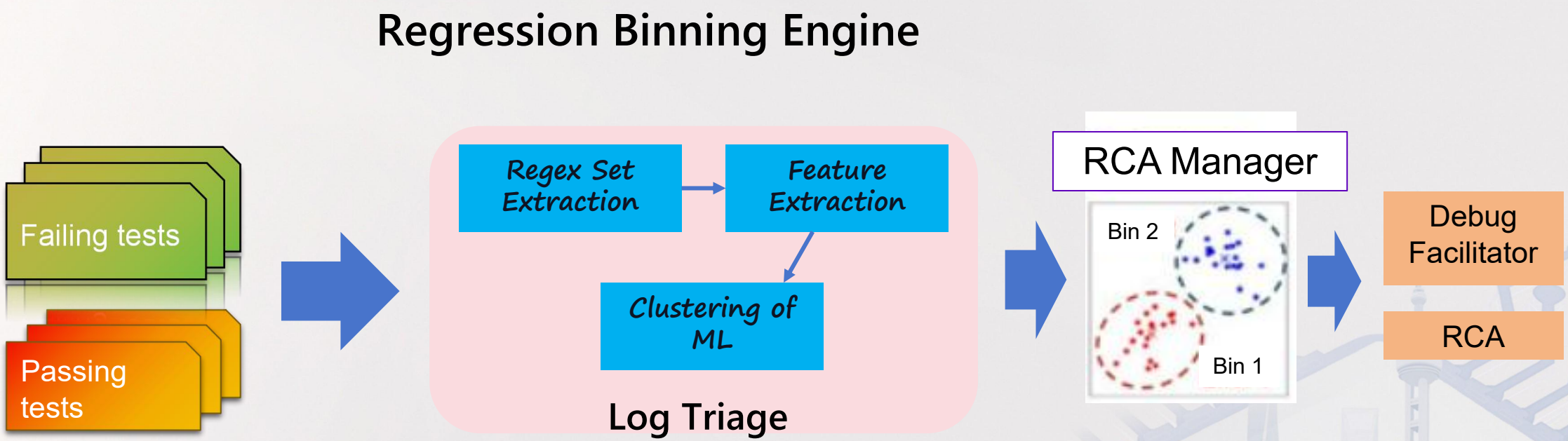
Regression Debug Flow with ML



Regression Binning

Regression Binning with ML

- Perform failure clustering based on the similarity of simulation logs



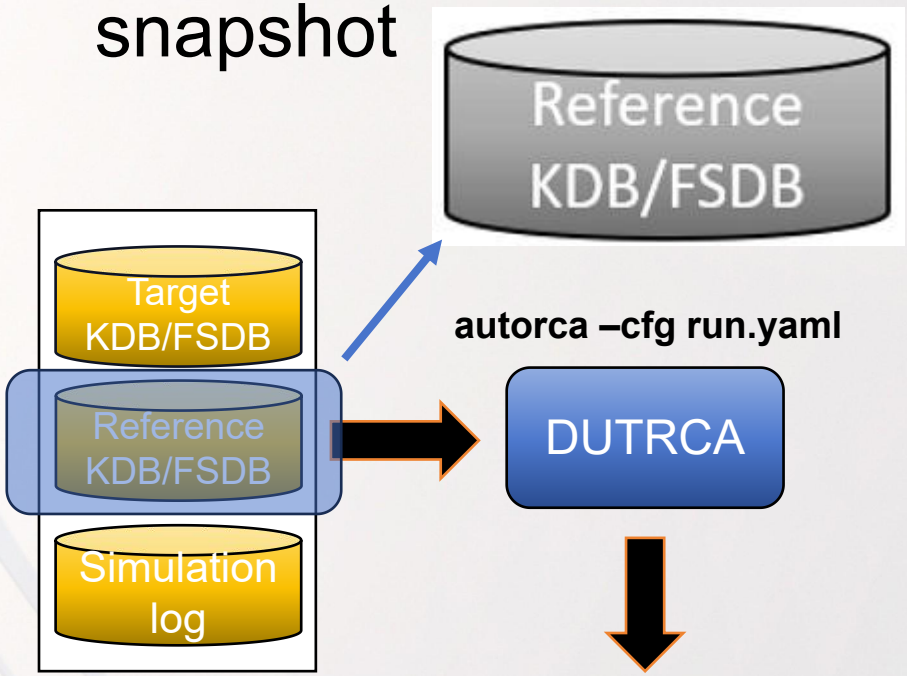
Useful Regression Binning Features

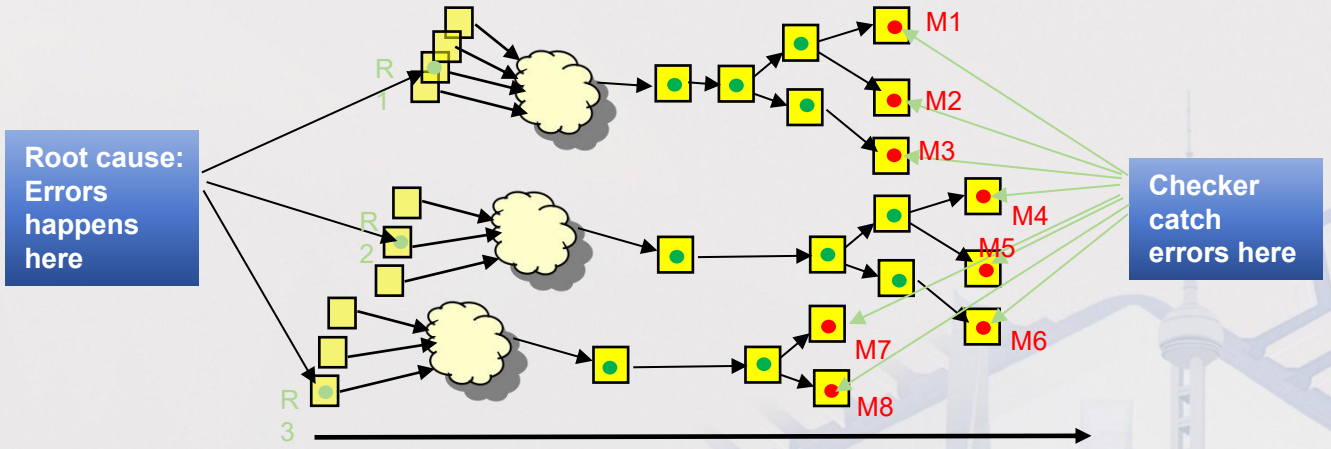
- Predefined Errors
  - UVM Errors, OVM Errors, SVA Failures, etc.
- User Defined Errors
  - Control the Message Chosen Mechanism
    - Filter Rules
    - Waive Rules
    - Rule Priority
  - Adjust the Binning Result
    - Replace Rule
- Multiple-Error Binning

Bug Prediction

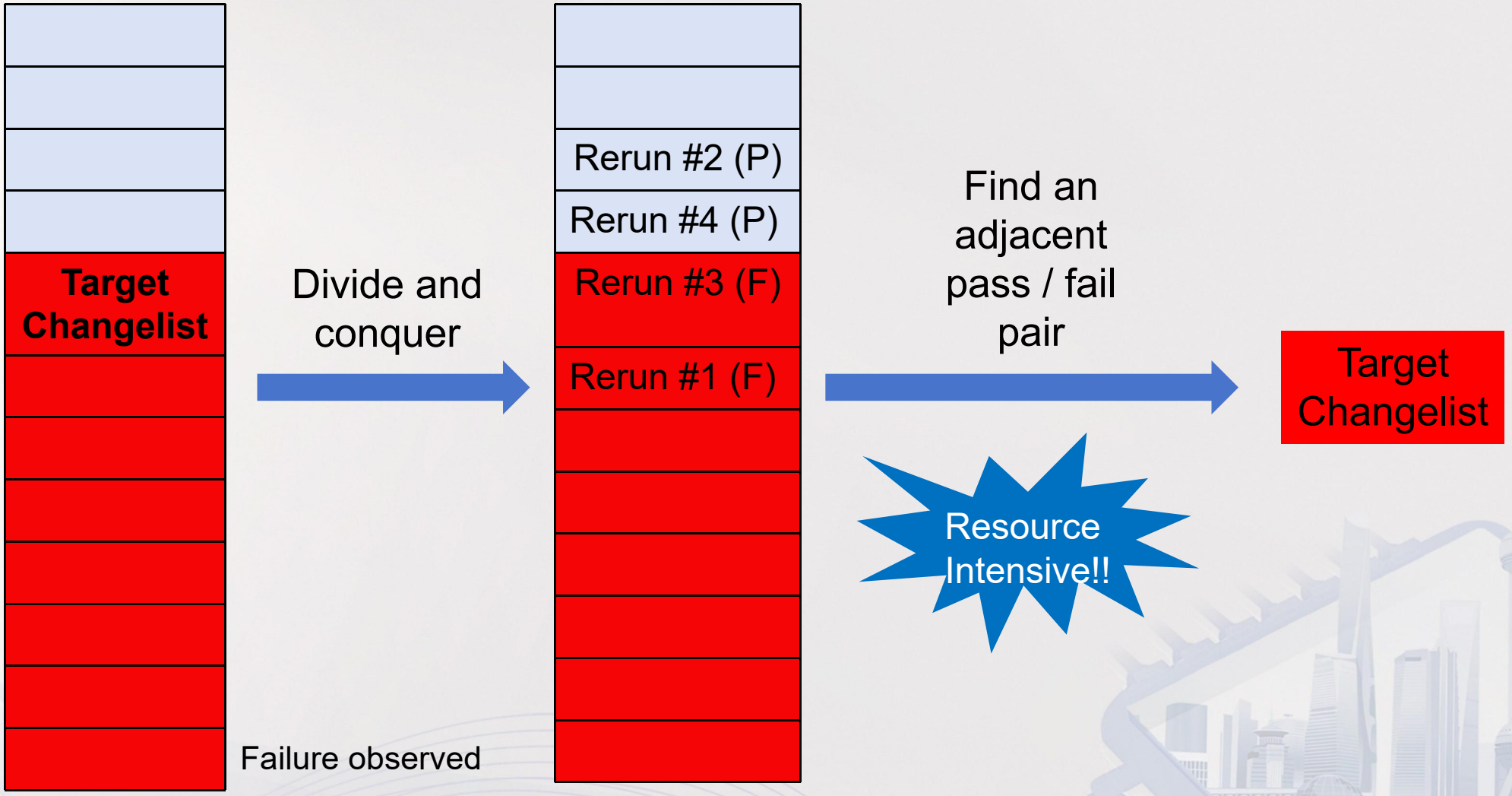
Probe Engine

- Some debug engines need a reference design snapshot
- We need a probe engine to find the target/reference design snapshot



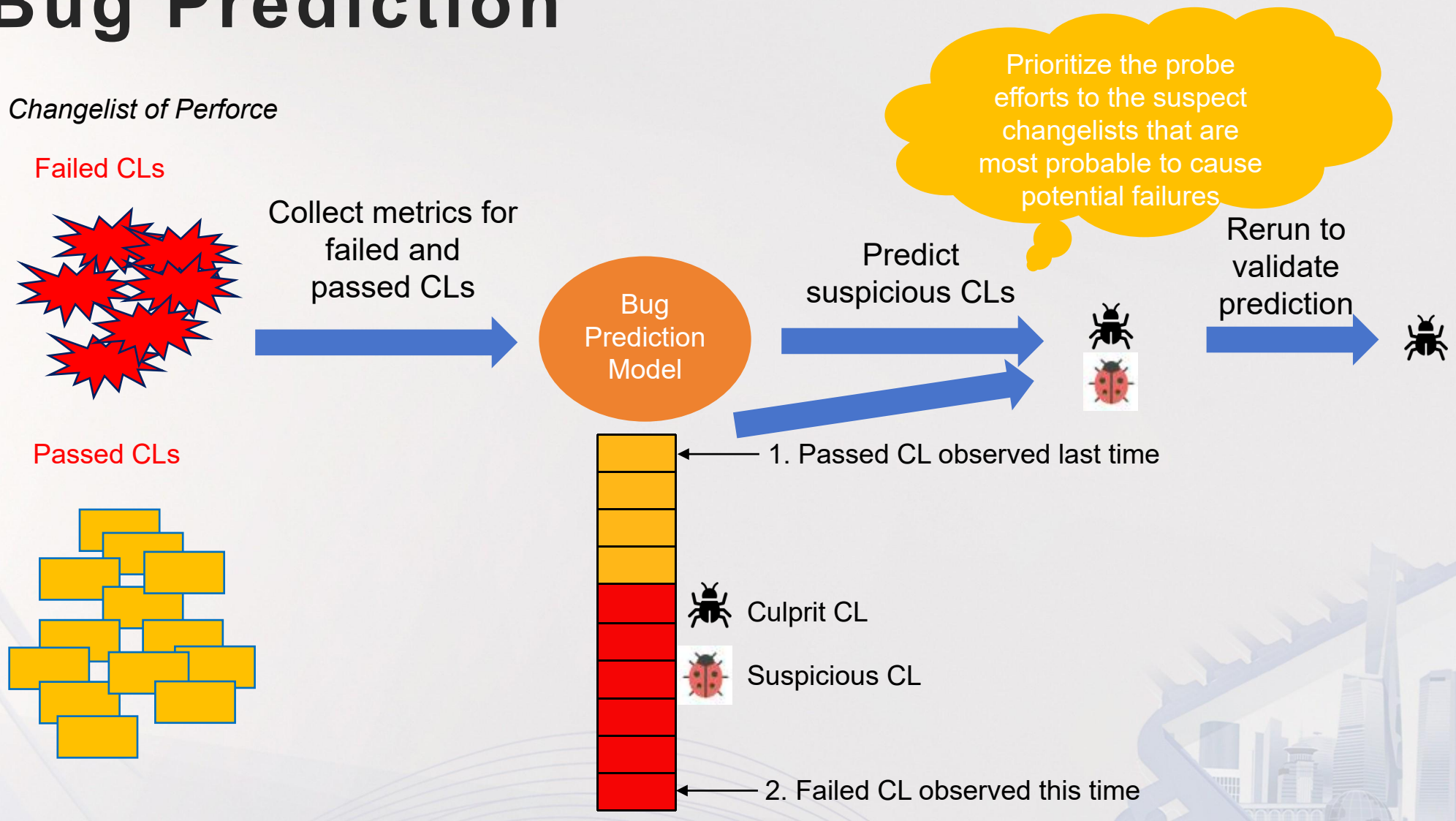


Traditional Probe without Bug Prediction



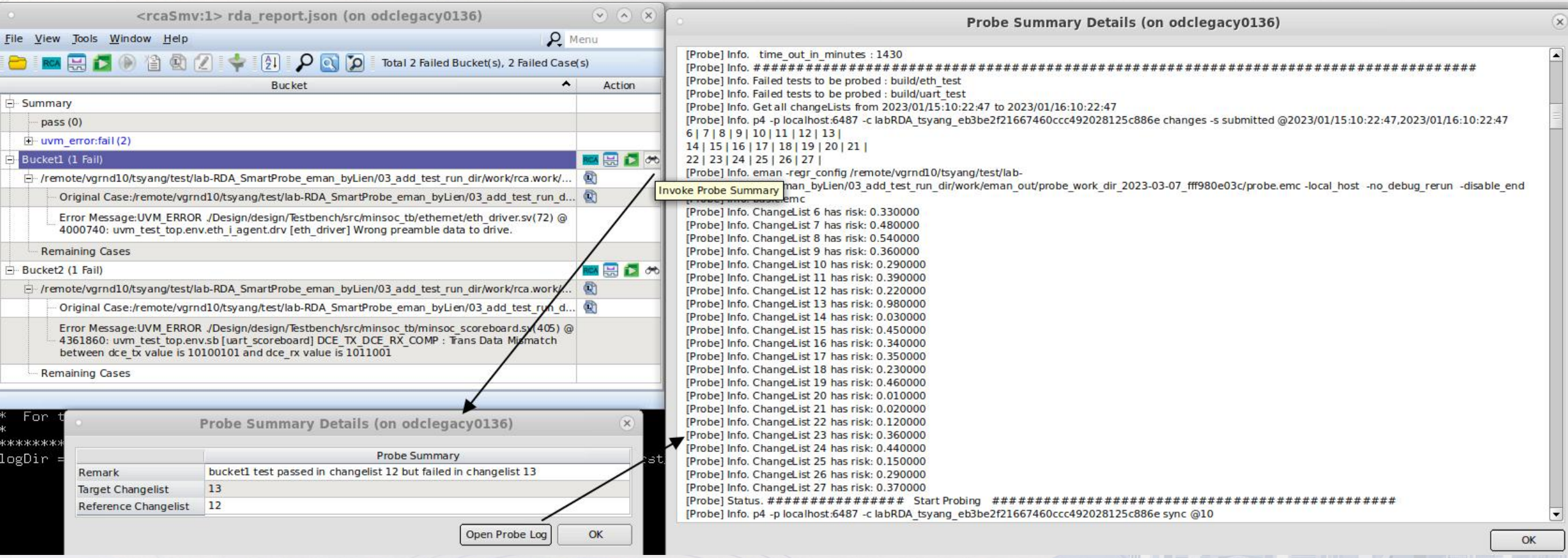
Bug Prediction

CL: Changelist of Perforce



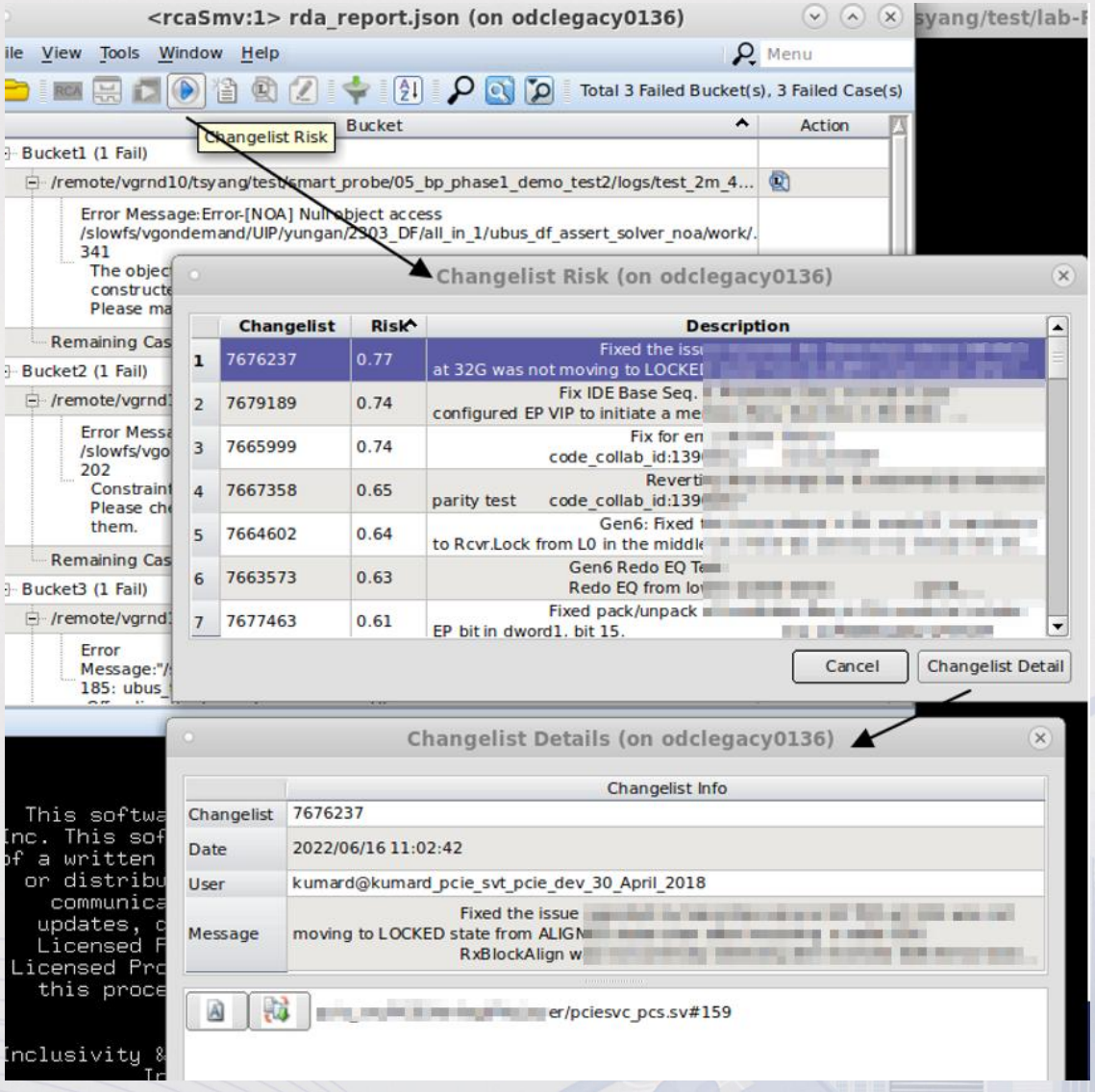
Bug Prediction for Smart Probe

- Prioritize the probe efforts to high-risk changelists



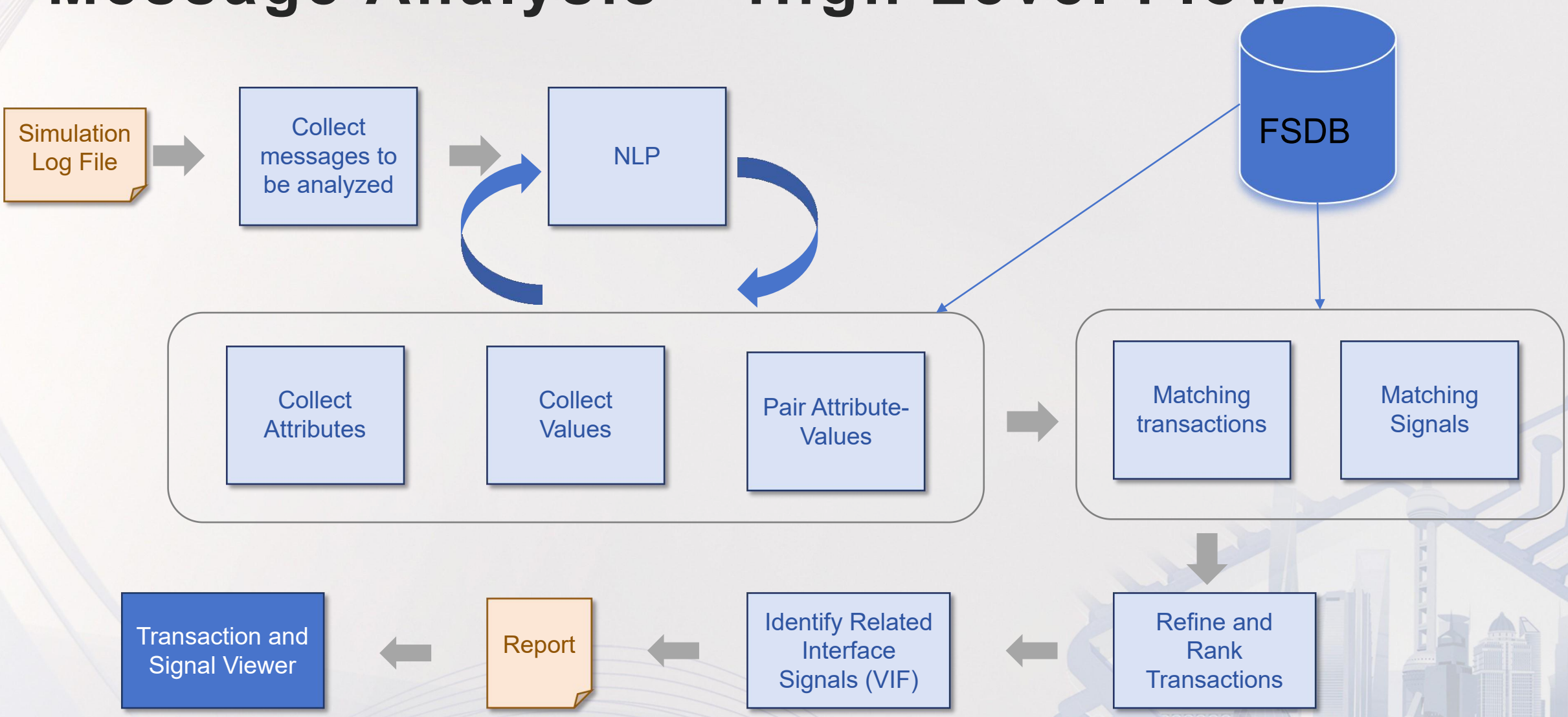
Bug Prediction for Risk Assessment

- Help the users assess high-risk changelists without running probe



Message Analysis

Message Analysis – High Level Flow

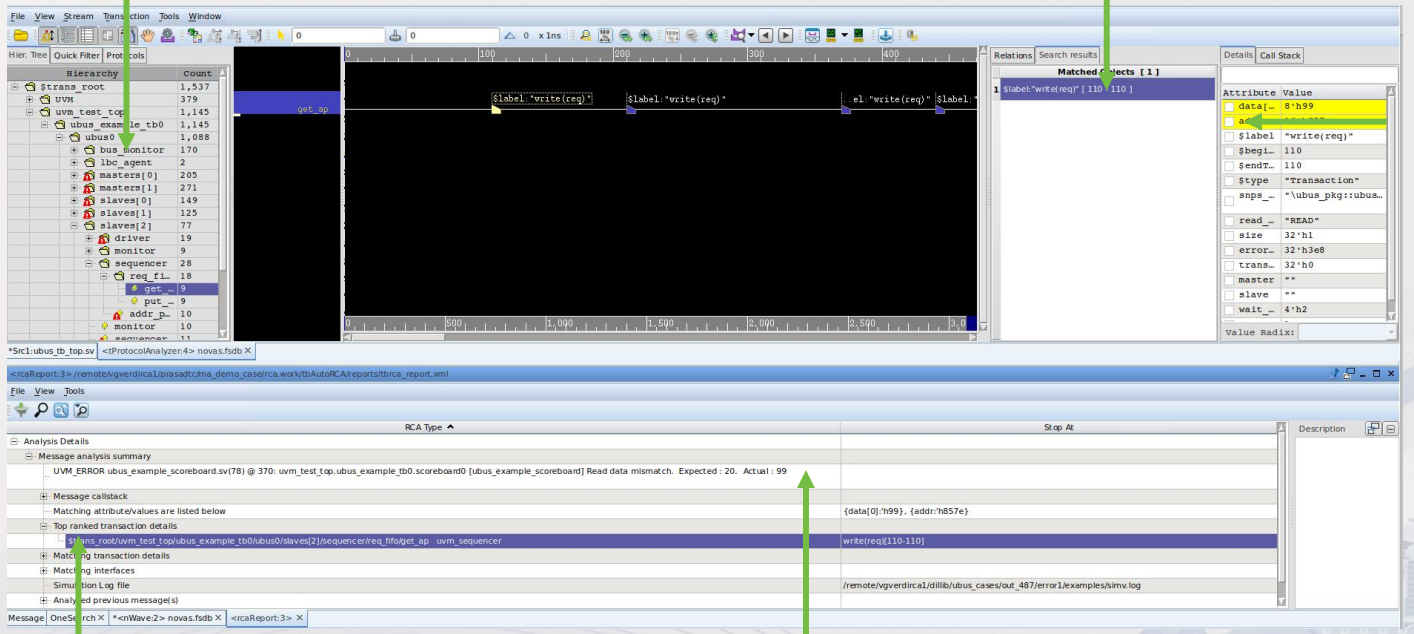


Message Analysis – Example

```
TBAR_INFO: Started analyzing debug message(s) from simulation log file {/remote/vgsource12/ikshvaku/TD.VERDI_REG/unit_VERDI/unittest/evProds/tbAutoRCA/testData/swayCases/TB_ERRROR/out_230/examples/simv.log}
TBAR_INFO: Simulation log file contains ERRORS(14) debug messages.
TBAR_INFO: Analyzing the first ERROR log message.
TBAR_INFO: Analyzing the below log message.
    {UVM_ERROR ubus_example_master_seq_lib.sv(206) @ 80: uvm_test_top.ubus_example_tb0.ubus0.masters[1].sequencer@@loop_read_modify_write_seq.rmw_seq [read_modify_write_seq]
loop_read_modify_write_seq.rmw_seq Read Modify Write Read error!}
TBAR_INFO: Completed analyzing debug message(s) from simulation log file.
TBAR_INFO: Matching attribute/values are listed below.
TBAR_INFO:   {addr:020a}, {data[0]:e9}
TBAR_INFO: Matching transactions after analyzing actual, next and previous messages are listed below
TBAR_INFO:   Stream: {$trans_root/uvm_test_top/ubus_example_tb0/ubus0/masters[1]/driver/seq_item_port} Matching transactions: {2}
TBAR_INFO:   Stream: {$trans_root/uvm_test_top/ubus_example_tb0/ubus0/masters[1]/sequencer} Matching transactions: {1}
TBAR_INFO: Total matching transactions {3}
TBAR_INFO: Matching virtual interface paths are listed below
TBAR_INFO:   /ubus_tb_top/vif  Signals: {sig_read,sig_write,sig_addr}
TBAR_INFO: Top ranked transaction details are listed below
TBAR_INFO:   Transaction {get_next_item(req)[80-80]} Stream {$trans_root/uvm_test_top/ubus_example_tb0/ubus0/masters[1]/driver/seq_item_port} Component type {uvm_driver} Port type {uvm_seq_item_pull_port}
TBAR_INFO:     Connected to {uvm_test_top.ubus_example_tb0.ubus0.masters[1].sequencer.seq_item_export} Component type {uvm_sequencer} Port type {uvm_seq_item_pull_imp}
TBAR_INFO: Please run the {/slowfs/vgvips19/prasadtc/verdiLog/tbAutoRCA/reports//simvErrorAnalysisLog/run_verdi} script to view the simv log file analysis results in Verdi.
```

Larger set of transactions

Smaller set of Related transactions



Interested transaction attributes

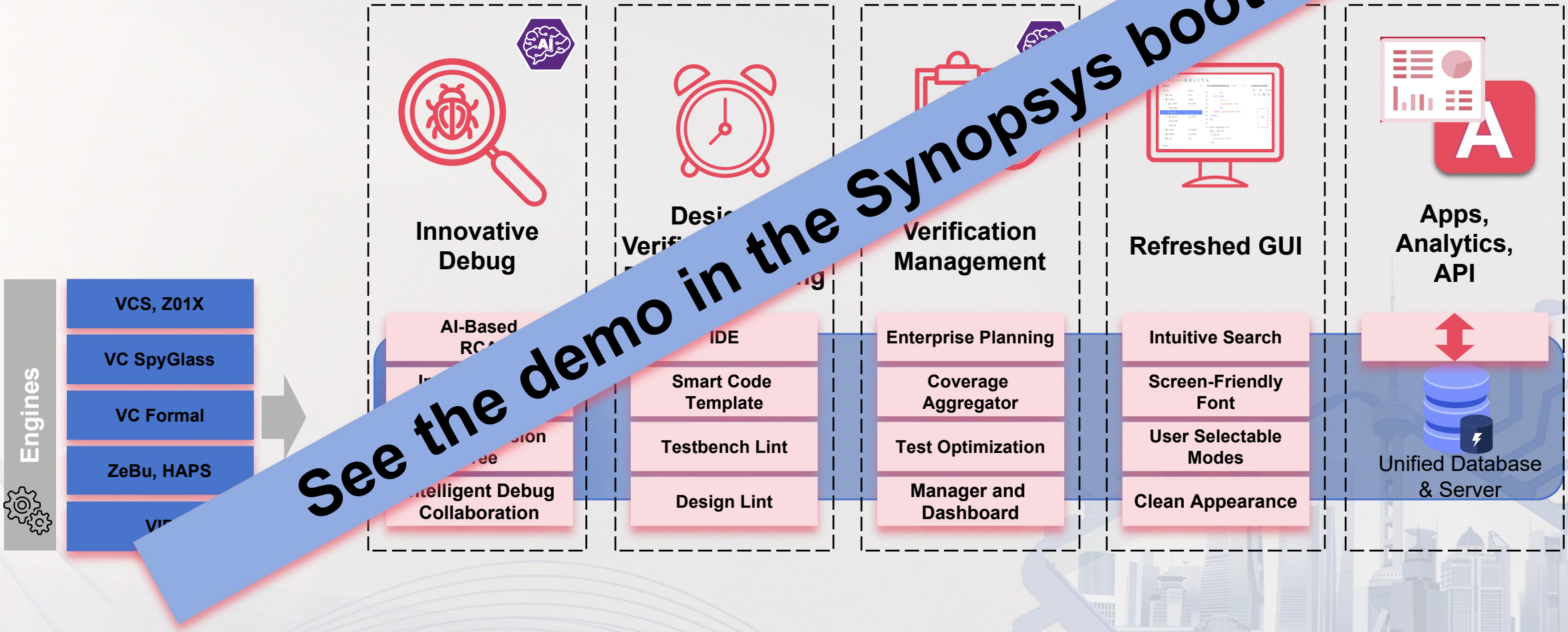
Matching transaction details

Simulation log message

Summary

- Manual regression debug is tedious, but we can automate it with AI and advanced RCA technologies
- Regression binning classifies many failed tests into a few bins of different errors
- Bug prediction reduces the time on locating target/reference snapshots for debug engines
- Message analysis identifies transactions that are related to the error message

Introducing Next-Generation Verdi Platfor



Questions