



DESIGN AND VERIFICATION™ CONFERENCE AND EXHIBITION

Shanghai | September 20, 2023



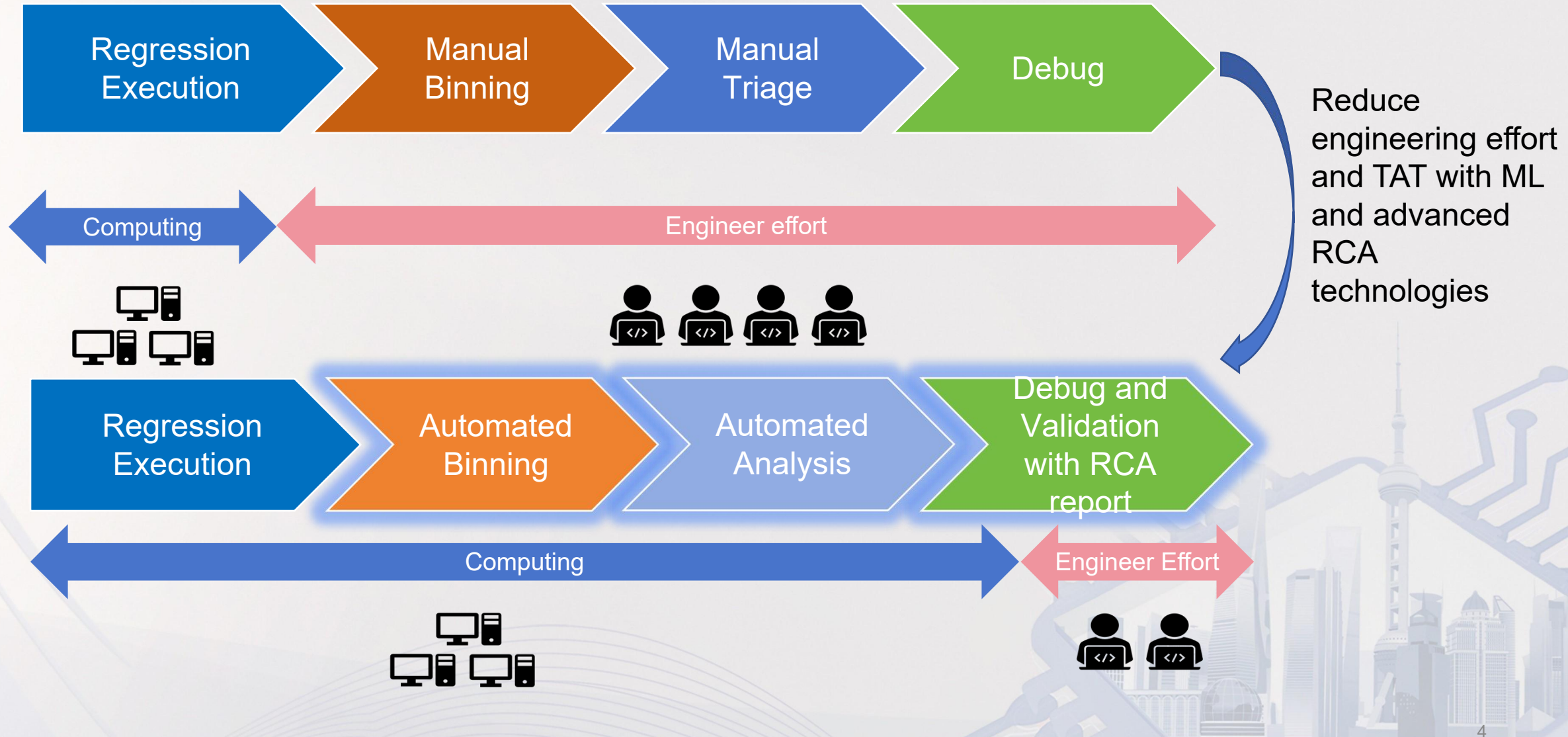
Debug Automation with AI

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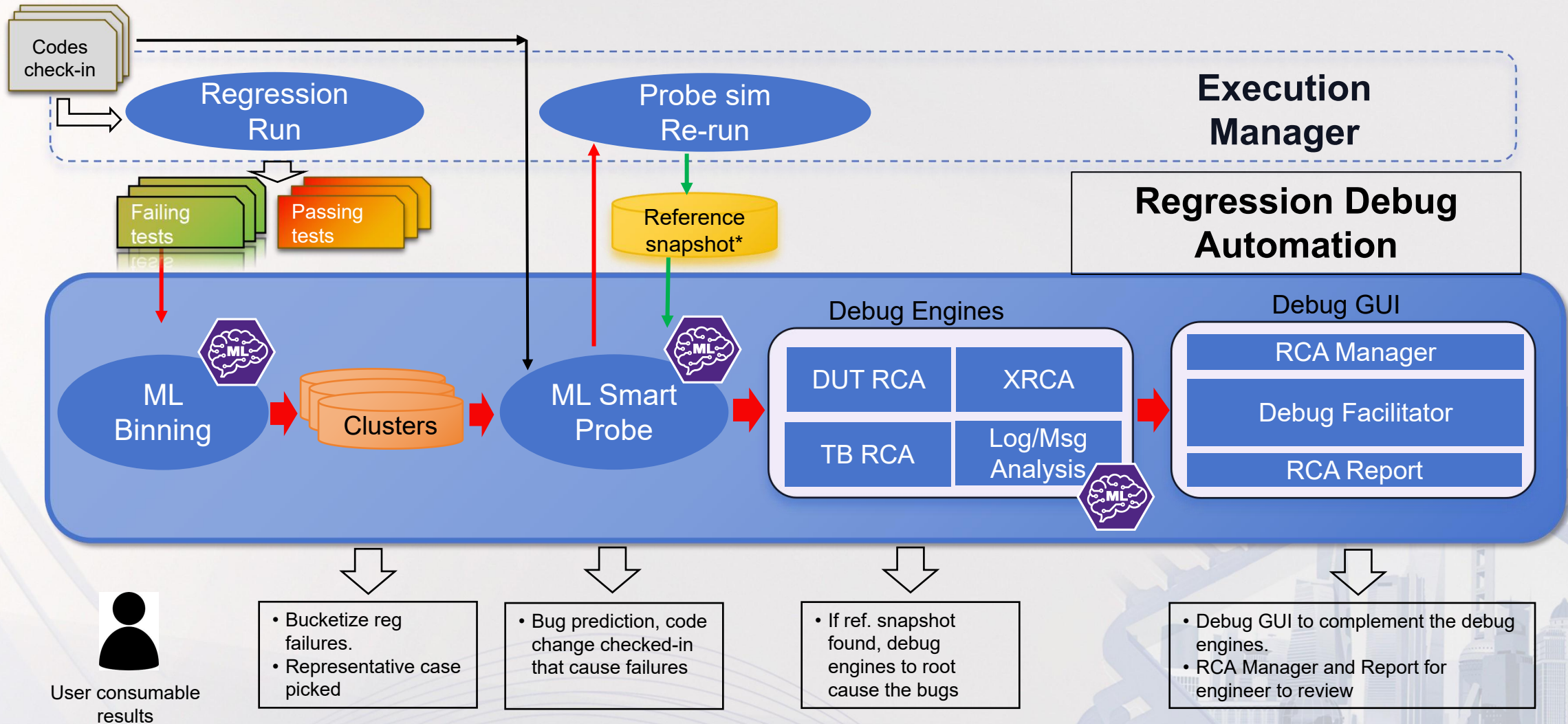


Motivation and Debug Flow

Regression Debug Automation Motivation



Regression Debug Flow with ML

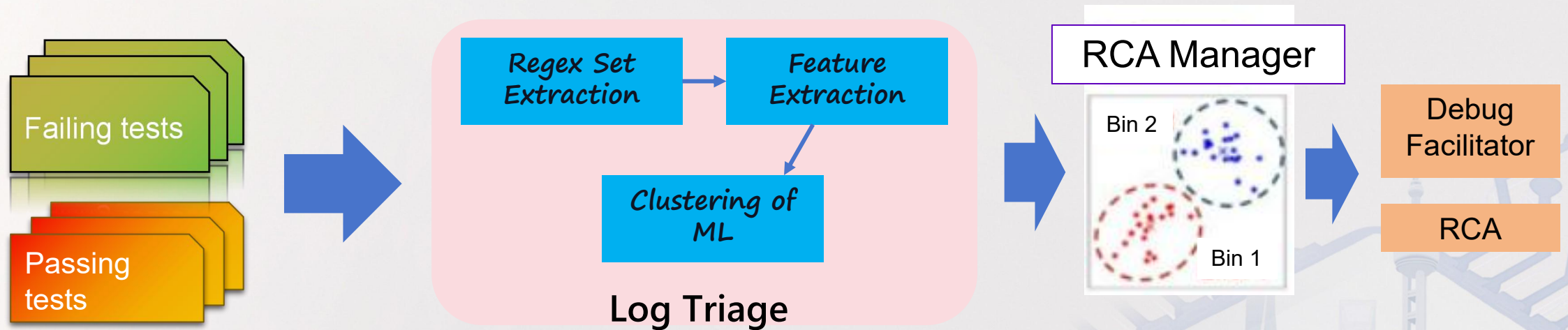


Regression Binning

Regression Binning with ML

- Perform failure clustering based on the similarity of simulation logs

Regression Binning Engine



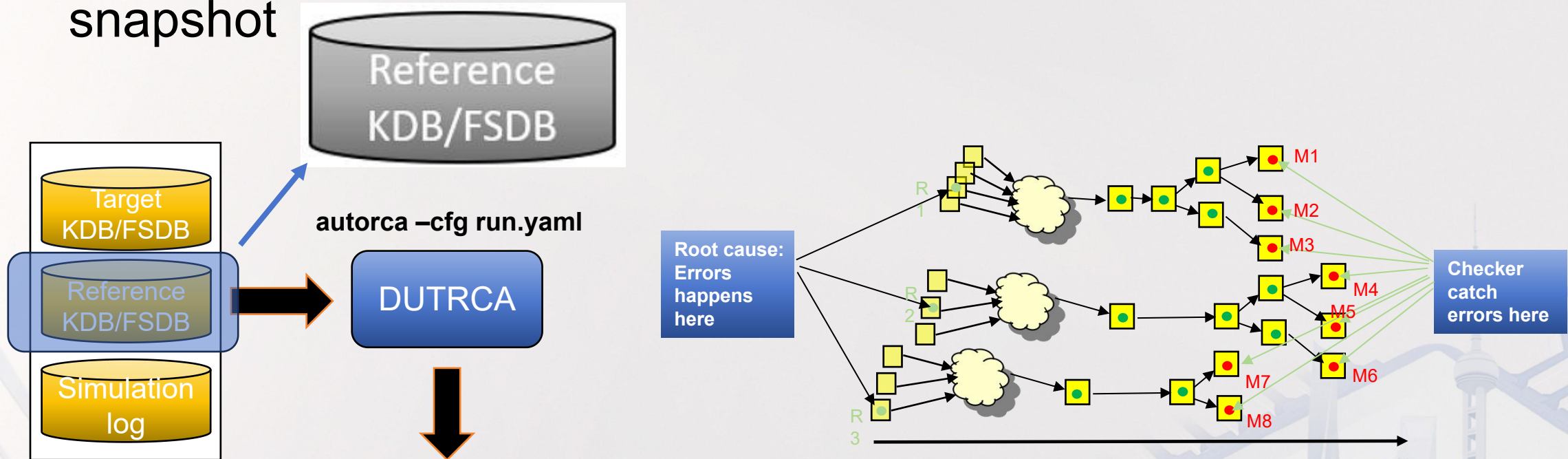
Useful Regression Binning Features

- Predefined Errors
 - UVM Errors, OVM Errors, SVA Failures, etc.
- User Defined Errors
 - Control the Message Chosen Mechanism
 - Filter Rules
 - Waive Rules
 - Rule Priority
 - Adjust the Binning Result
 - Replace Rule
- Multiple-Error Binning

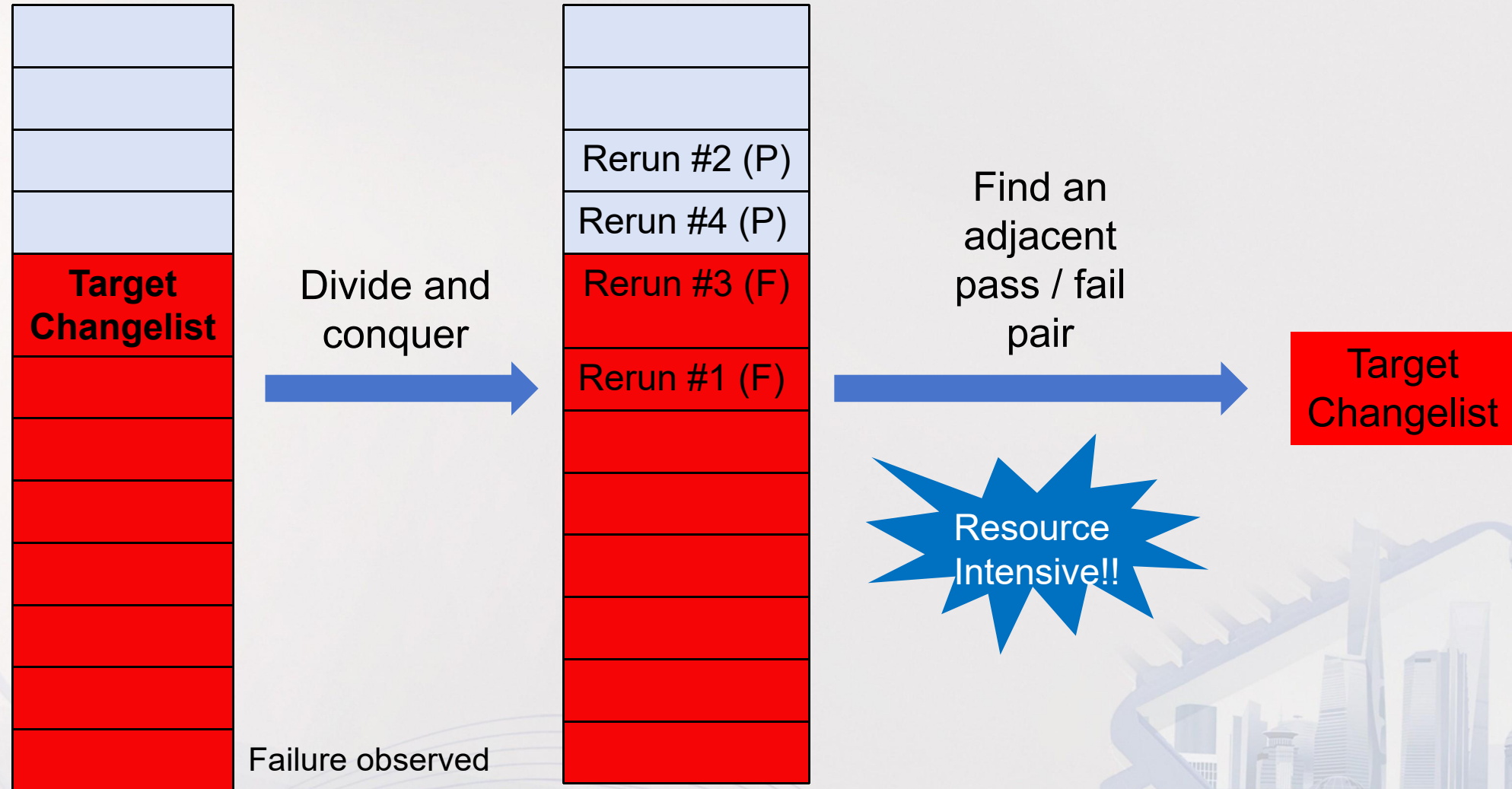
Bug Prediction

Probe Engine

- Some debug engines need a reference design snapshot
- We need a probe engine to find the target/reference design snapshot

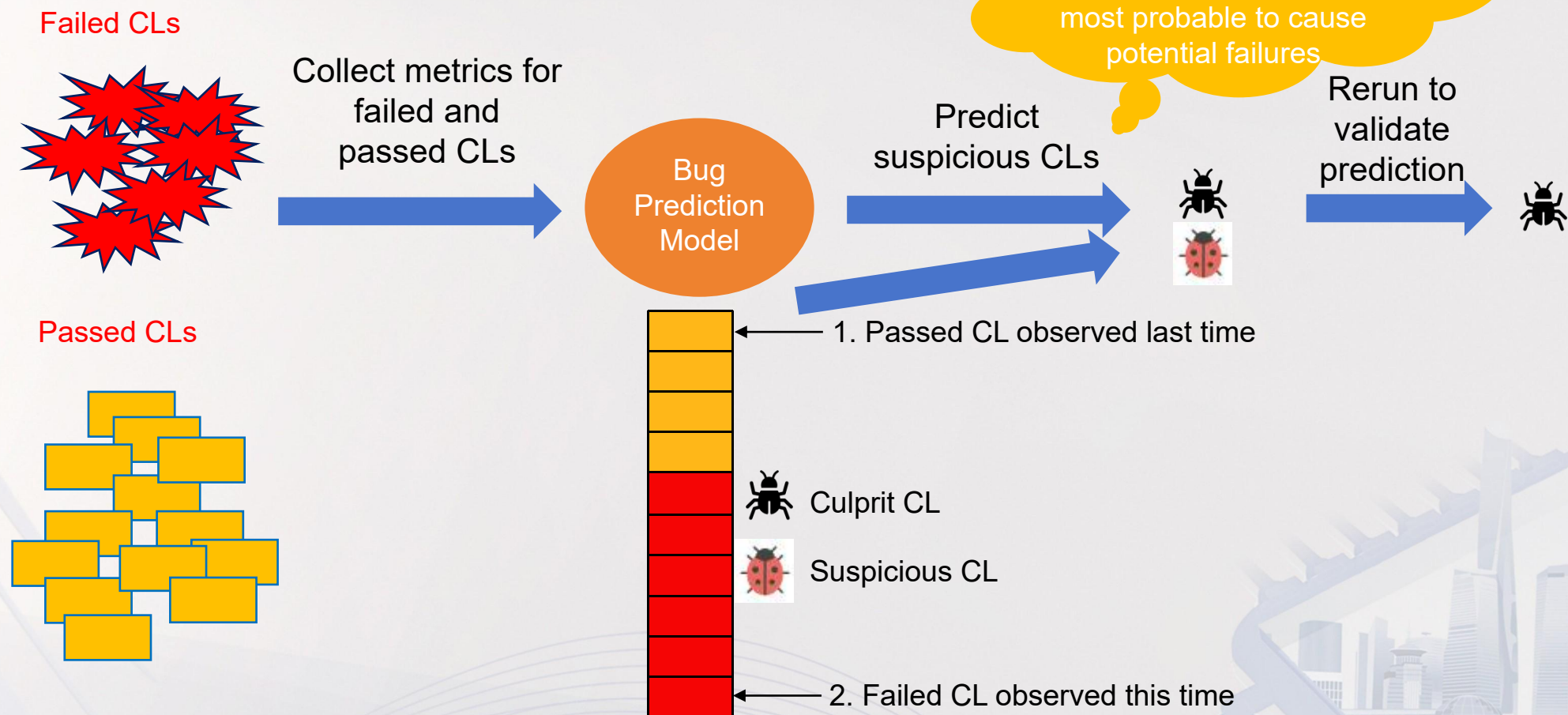


Traditional Probe without Bug Prediction



Bug Prediction

CL: Changelist of Perforce



Bug Prediction for Smart Probe

- Prioritize the probe efforts to high-risk changelists

The screenshot displays the Smart Probe application interface, which is used for managing and analyzing test results. The main window, titled "<rcaSmv:1> rda_report.json (on odclegacy0136)", shows a list of test buckets. The "Bucket1 (1 Fail)" is selected, showing details for a failed test case. An arrow points from the "Invoke Probe Summary" button in the "Bucket1 (1 Fail)" section to a secondary window titled "Probe Summary Details (on odclegacy0136)".

The "Probe Summary Details" window provides a comprehensive overview of the test results, including a list of changelists and their associated risk scores. The risk scores are calculated based on the test results, with higher scores indicating higher risk. The summary also includes a table of test results, showing the status of each test case across different changelists.

Probe Summary Details (on odclegacy0136)

[Probe] Info. time_out_in_minutes : 1430
[Probe] Info. #####
[Probe] Info. Failed tests to be probed : build/eth_test
[Probe] Info. Failed tests to be probed : build/uart_test
[Probe] Info. Get all changeLists from 2023/01/15:10:22:47 to 2023/01/16:10:22:47
[Probe] Info. p4 -p localhost:6487 -c labRDA_tsyang_eb3be2f21667460ccc492028125c886e changes -s submitted @2023/01/15:10:22:47,2023/01/16:10:22:47
6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 |
22 | 23 | 24 | 25 | 26 | 27 |
[Probe] Info. eman -regr_config /remote/vgrnd10/tsyang/test/lab-
[Probe] Info. eman_byLien/03_add_test_run_dir/work/eman_out/probe_work_dir_2023-03-07_fff980e03c/probe.emc -local_host -no_debug_rerun -disable_end

[Probe] Info. ChangeList 6 has risk: 0.330000
[Probe] Info. ChangeList 7 has risk: 0.480000
[Probe] Info. ChangeList 8 has risk: 0.540000
[Probe] Info. ChangeList 9 has risk: 0.360000
[Probe] Info. ChangeList 10 has risk: 0.290000
[Probe] Info. ChangeList 11 has risk: 0.390000
[Probe] Info. ChangeList 12 has risk: 0.220000
[Probe] Info. ChangeList 13 has risk: 0.980000
[Probe] Info. ChangeList 14 has risk: 0.030000
[Probe] Info. ChangeList 15 has risk: 0.450000
[Probe] Info. ChangeList 16 has risk: 0.340000
[Probe] Info. ChangeList 17 has risk: 0.350000
[Probe] Info. ChangeList 18 has risk: 0.230000
[Probe] Info. ChangeList 19 has risk: 0.460000
[Probe] Info. ChangeList 20 has risk: 0.010000
[Probe] Info. ChangeList 21 has risk: 0.020000
[Probe] Info. ChangeList 22 has risk: 0.120000
[Probe] Info. ChangeList 23 has risk: 0.360000
[Probe] Info. ChangeList 24 has risk: 0.440000
[Probe] Info. ChangeList 25 has risk: 0.150000
[Probe] Info. ChangeList 26 has risk: 0.290000
[Probe] Info. ChangeList 27 has risk: 0.370000
[Probe] Status. ##### Start Probing #####
[Probe] Info. p4 -p localhost:6487 -c labRDA_tsyang_eb3be2f21667460ccc492028125c886e sync @10

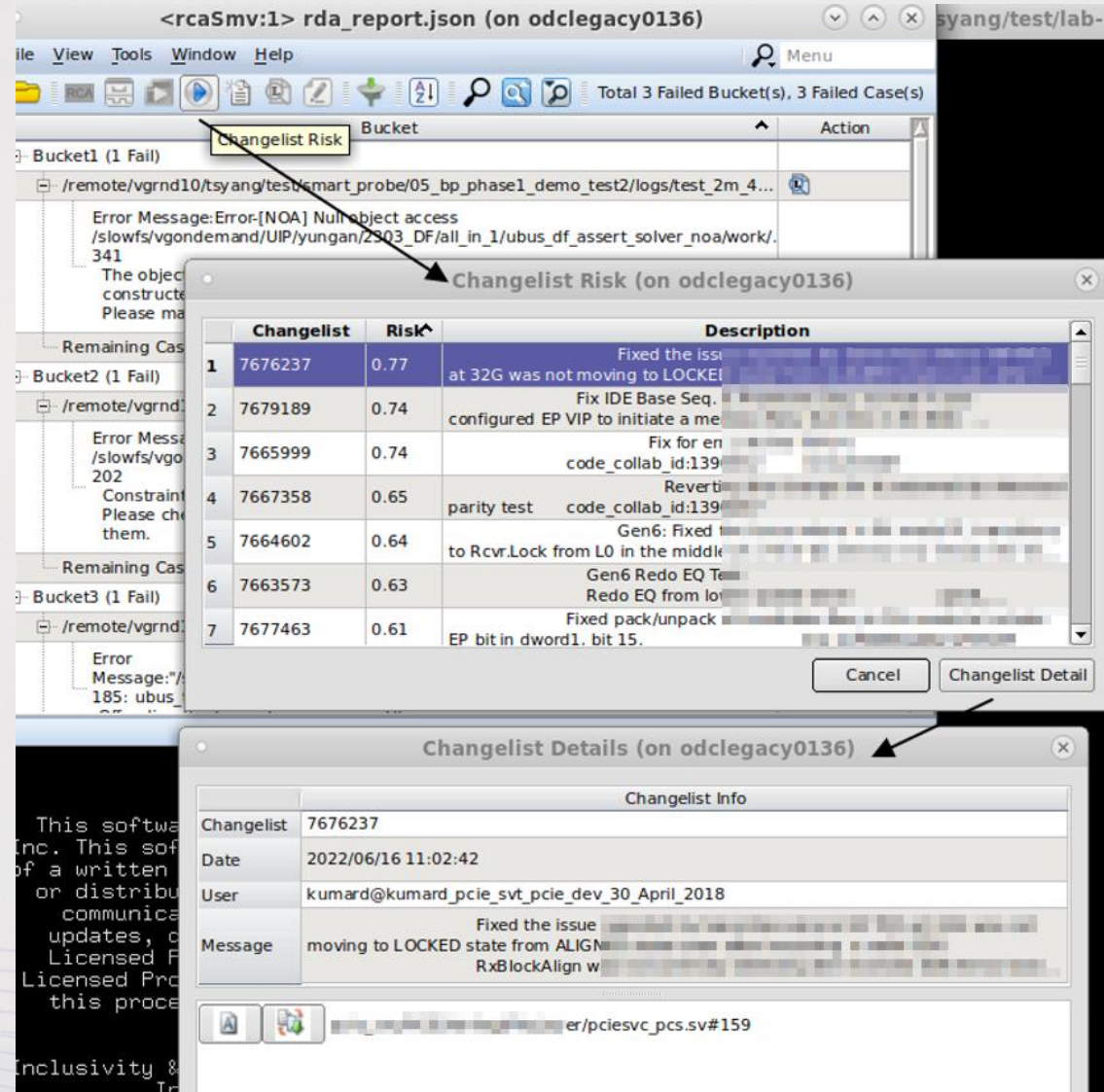
Probe Summary

Probe Summary	
Remark	bucket1 test passed in changelist 12 but failed in changelist 13
Target Changelist	13
Reference Changelist	12

Open Probe Log OK

Bug Prediction for Risk Assessment

- Help the users assess high-risk changelists without running probe



The screenshot shows a software interface for bug prediction and risk assessment. The main window displays a list of failed buckets and cases. A 'Changelist Risk' dialog box is open, showing a table of changelists with their risk scores and descriptions. A 'Changelist Details' dialog box is also open, providing more information about a specific changelist.

Changelist Risk (on odclegacy0136)

Changelist	Risk	Description
1 7676237	0.77	Fixed the issue at 32G was not moving to LOCKED state
2 7679189	0.74	Fix IDE Base Seq. configured EP VIP to initiate a message
3 7665999	0.74	Fix for error code_collab_id:139
4 7667358	0.65	Reverting parity test code_collab_id:139
5 7664602	0.64	Gen6: Fixed issue to Rcvr.Lock from L0 in the middle
6 7663573	0.63	Gen6 Redo EQ Timeout Redo EQ from local
7 7677463	0.61	Fixed pack/unpack EP bit in dword1, bit 15.

Changelist Details (on odclegacy0136)

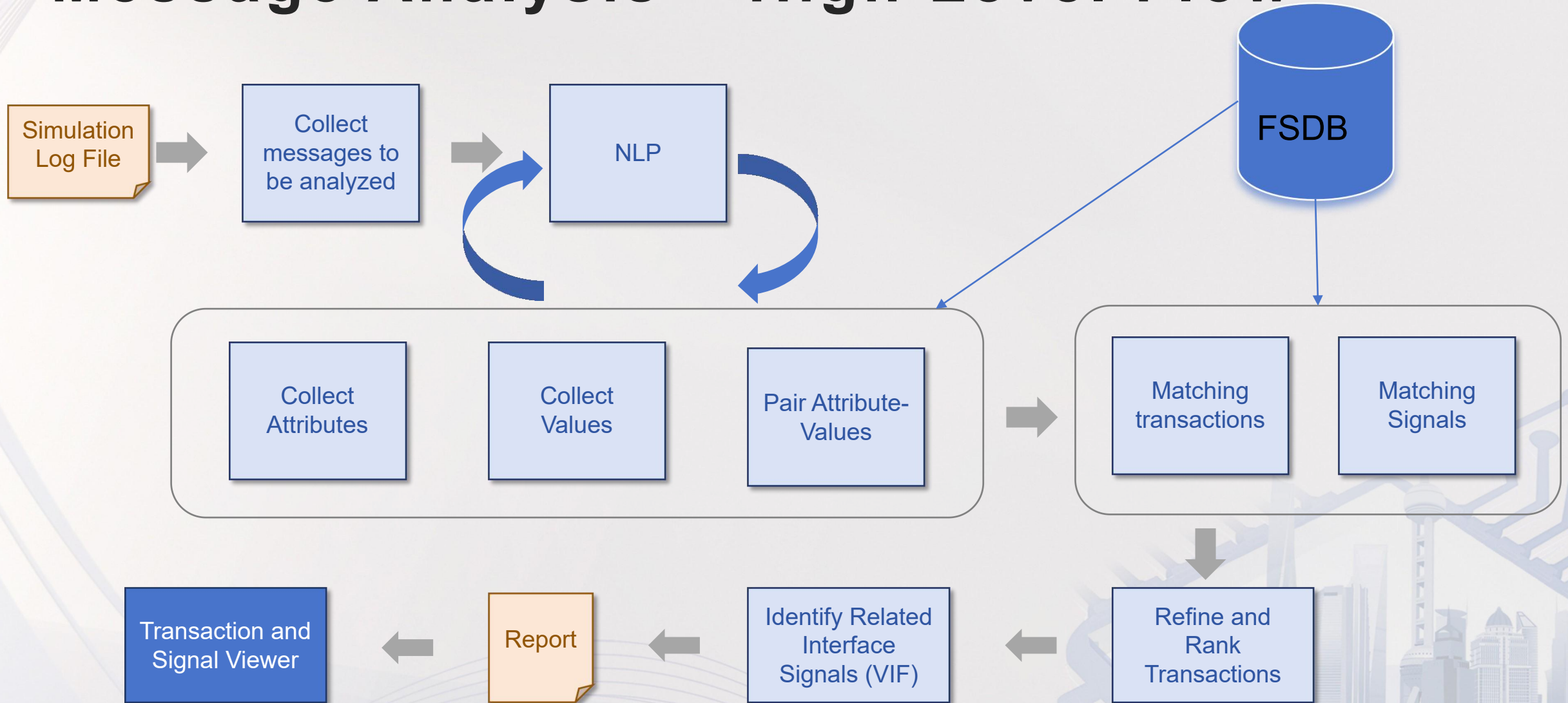
Changelist Info

Changelist	7676237
Date	2022/06/16 11:02:42
User	kumard@kumard_pcie_svt_pcie_dev_30_April_2018
Message	Fixed the issue moving to LOCKED state from ALIGN RxBlockAlign with

er/pciesvc_pcs.sv#159

Message Analysis

Message Analysis – High Level Flow



Message Analysis – Example

```
TBAR INFO: Started analyzing debug message(s) from simulation log file {/remote/vgsource12/ikshvaku/TD.VERDI_REG/unit_VERDI/unittest/evProds/tbAutoRCA/testData/swayCases/TB_ERROR/out_230/examples/simv.log}
TBAR INFO: Simulation log file contains ERRORS(14) debug messages.
TBAR INFO: Analyzing the first ERROR log message.
TBAR INFO: Analyzing the below log message.
{UVM_ERROR ubus_example_master_seq.lib.sv(206) @ 80: uvm_test_top.ubus_example_tb0.ubus0.masters[1].sequencer@loop_read_modify_write_seq.rmw_seq [read_modify_write_seq]
loop_read_modify_write_seq.rmw_seq Read Modify Write Read error!}
TBAR INFO: Completed analyzing debug message(s) from simulation log file.
TBAR INFO: Matching attribute/values are listed below.
TBAR INFO: {addr:020a}, {data[0]:e9}
TBAR INFO: Matching transactions after analyzing actual, next and previous messages are listed below
TBAR INFO: Stream: {$trans_root/uvm_test_top/ubus_example_tb0/ubus0/masters[1]/driver/seq_item_port} Matching transactions: {2}
TBAR INFO: Stream: {$trans_root/uvm_test_top/ubus_example_tb0/ubus0/masters[1]/sequencer} Matching transactions: {1}
TBAR INFO: Total matching transactions {3}
TBAR INFO: Matching virtual interface paths are listed below
TBAR INFO: /ubus tb top/vif Signals: {sig read,sig write,sig addr}
TBAR INFO: Top ranked transaction details are listed below
TBAR INFO: Transaction {get_next_item(req)[80-80]} Stream {$trans_root/uvm_test_top/ubus_example_tb0/ubus0/masters[1]/driver/seq_item_port} Component type {uvm driver} Port type {uvm_seq_item_pull_port}
TBAR INFO: Connected to {uvm_test_top.ubus_example_tb0.ubus0.masters[1].sequencer.seq_item_export} Component type {uvm sequencer} Port type {uvm_seq_item_pull_imp}
TBAR INFO: Please run the {/slowfs/vgvips19/prasadtc/verdiLog/tbAutoRCA/reports//simvErrorAnalysisLog/run_verdi} script to view the simv log file analysis results in Verdi.
```

Larger set of transactions

Smaller set of Related transactions

The screenshot displays the Verdi tool interface with several panels. The 'Hier. Tree' on the left shows a project hierarchy with components like 'uvm_test_top', 'ubus_example_tb0', and 'ubus0'. The central 'Stream' panel shows a timeline of transactions with labels like 'get_up', 'write(req)', and 'el "write(req)". The 'Relations' panel on the right shows 'Matched Objects (11)' with a table of attributes and values. The 'Details' panel on the far right shows a detailed view of a transaction with attributes like 'data', 'addr', 'type', 'size', 'error', 'trans', 'master', 'slave', and 'wait'. The bottom panel shows a list of transactions with columns for 'RCA Type', 'Stop At', and 'Description'. A green arrow points from the 'Larger set of transactions' text to the 'Stream' panel. Another green arrow points from the 'Smaller set of Related transactions' text to the 'Relations' panel. A third green arrow points from the 'Matching transaction details' text to the 'Details' panel. A fourth green arrow points from the 'Simulation log message' text to the bottom panel.

Attribute	Value
data	8'h99
addr	020a
label	"write(req)"
\$begi	110
\$send	110
\$type	"Transaction"
snps	"\ubus_pkg:ubus"
read	"READ"
size	32'h1
error	32'h3e8
trans	32'h0
master	**
slave	**
wait	4'h2

RCA Type	Stop At	Description
UVM_ERROR ubus_example_scoreboard.sv(78) @ 370: uvm_test_top.ubus_example_tb0.scoreboard0 [ubus_example_scoreboard] Read data mismatch. Expected : 20. Actual : 99		
Matching attribute/values are listed below		{data[0]:h99}, {addr:h057e}
Top ranked transaction details		
Stream: {\$trans_root/uvm_test_top/ubus_example_tb0/ubus0/slaves[2]/sequencer/req_fifo/get_ap [uvm_sequencer]		write(req)[110-110]
Matching transaction details		
Matching interfaces		
Simulation log file		/remote/vgveridical/dllib/ubus_cases/out_487/error1examples/simv.log

Interested transaction attributes

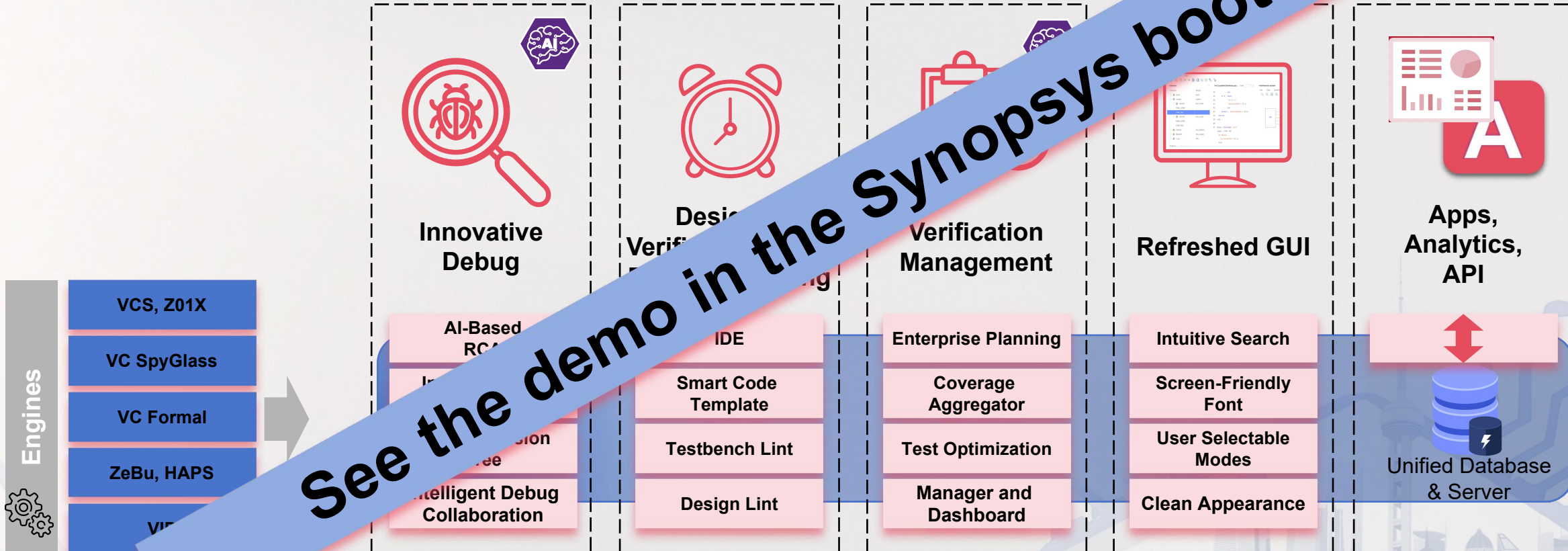
Matching transaction details

Simulation log message

Summary

- Manual regression debug is tedious, but we can automate it with AI and advanced RCA technologies
- **Regression binning** classifies many failed tests into a few bins of different errors
- **Bug prediction** reduces the time on locating target/reference snapshots for debug engines
- **Message analysis** identifies transactions that are related to the error message

Introducing Next-Generation Verdi Platform



Questions

