2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA

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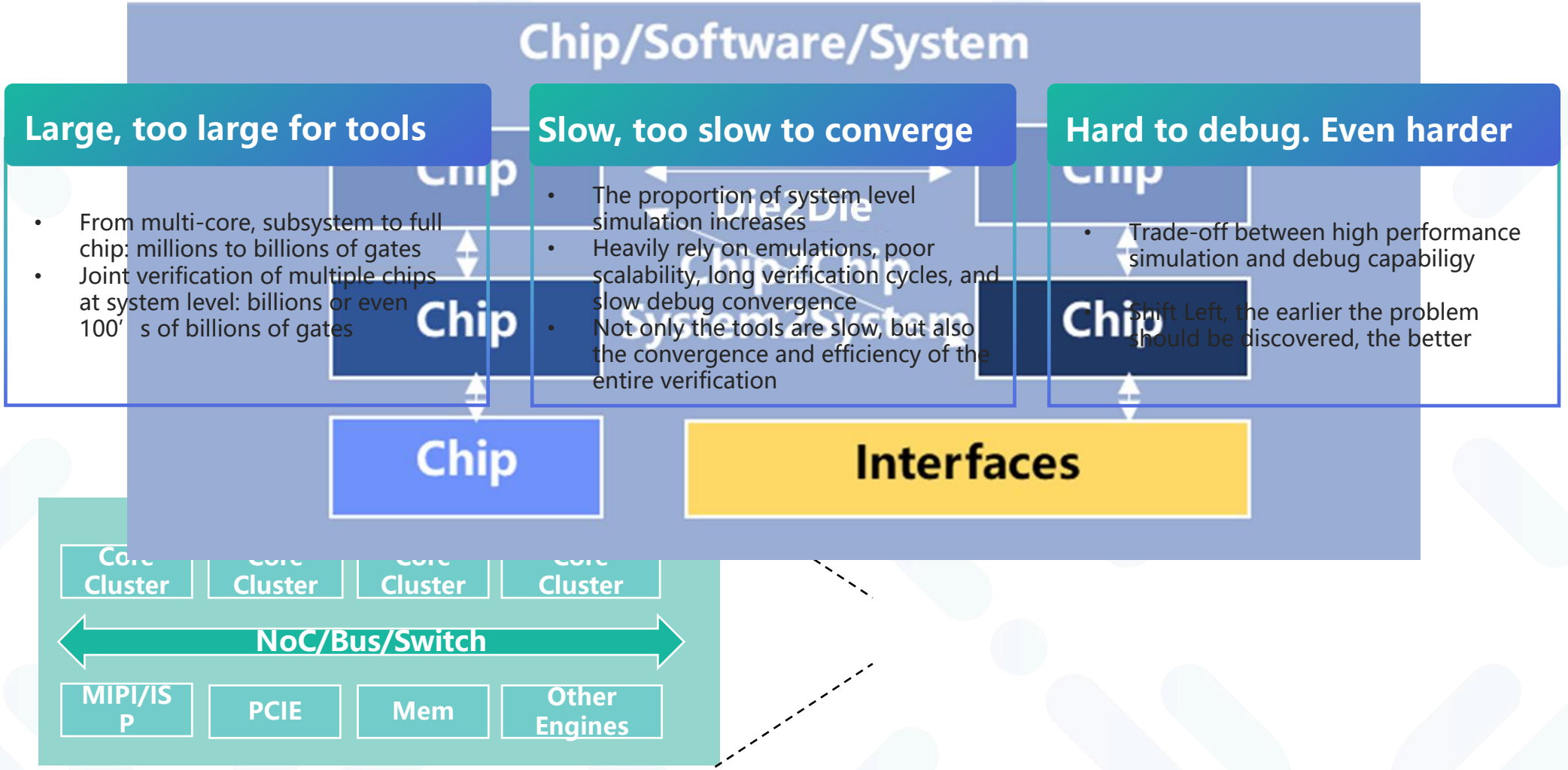
System Design with Agile Verification and Continuous Acceleration

Luke Yang
X-EPIC

Challenges in the Fast-growing System Design and Verification



What do System Companies need from EDA?
Faster, stronger verification systems

How System Companies are Re-shaping requirements for EDA

Several trend-related presentations highlighted the investments that hyperscale data center and systems companies are making in strengthening their SoC design teams in-house - e.g., Google, Meta, Microsoft, Amazon, etc.

The panel asked representatives from these companies - **"What do you need from EDA?" . Their answers can be summarized as follows, "Faster, stronger verification systems."**

How can Chip Design be Agile?

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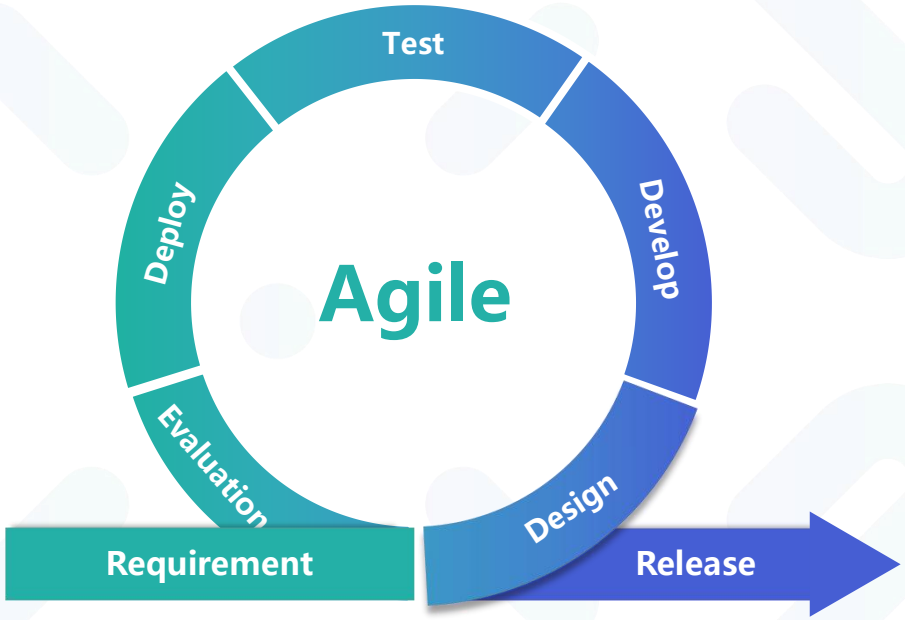
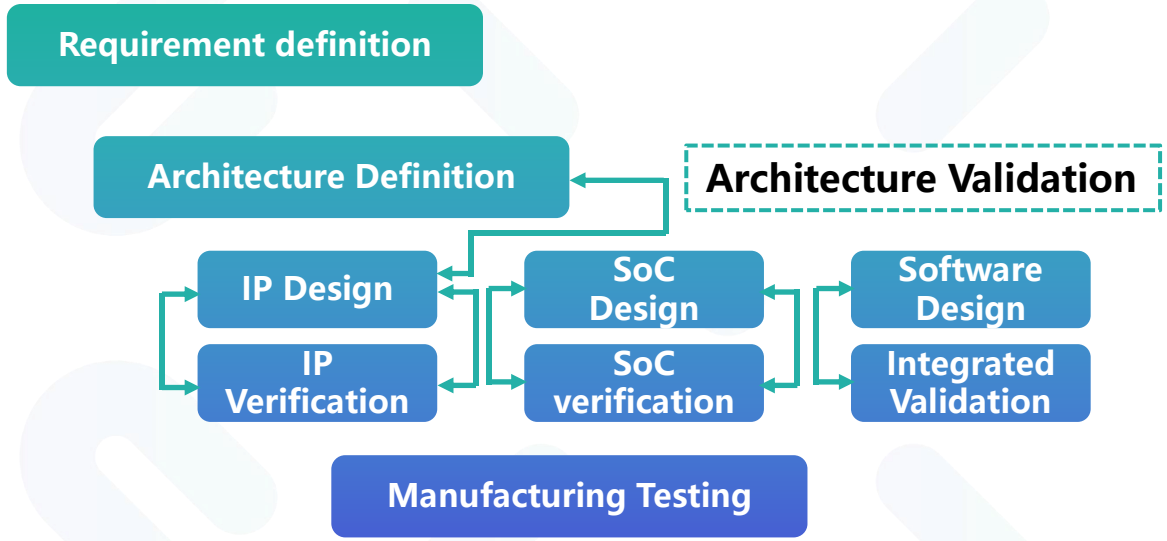
Software Design



- Quick respond to changes
- Continuous testing

Chip Design



A Long, step-after-step and high-cost journey

Our Answer：Agile Verification with Continuous Acceleration

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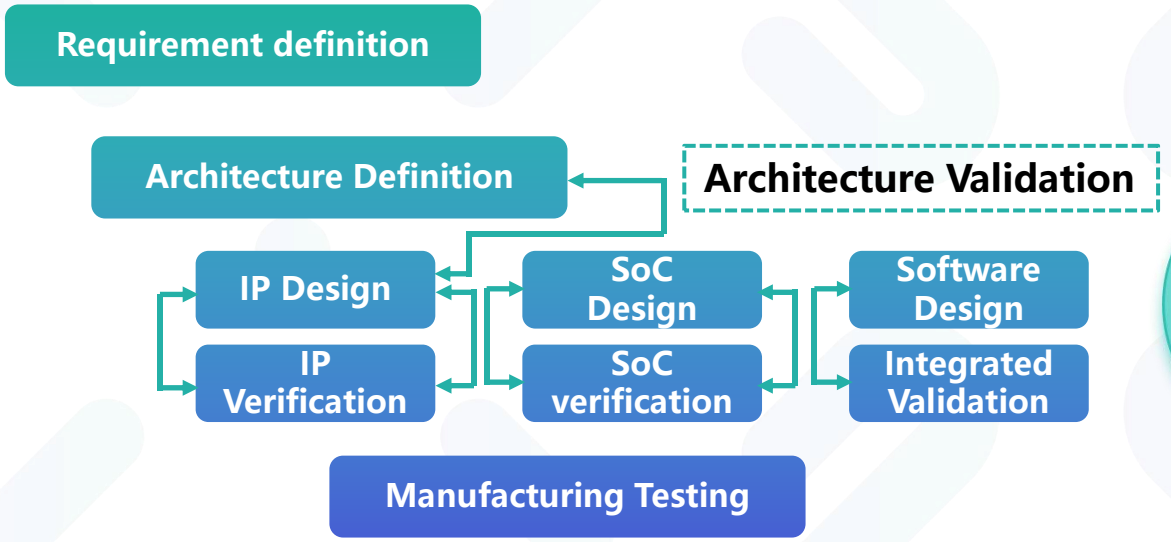

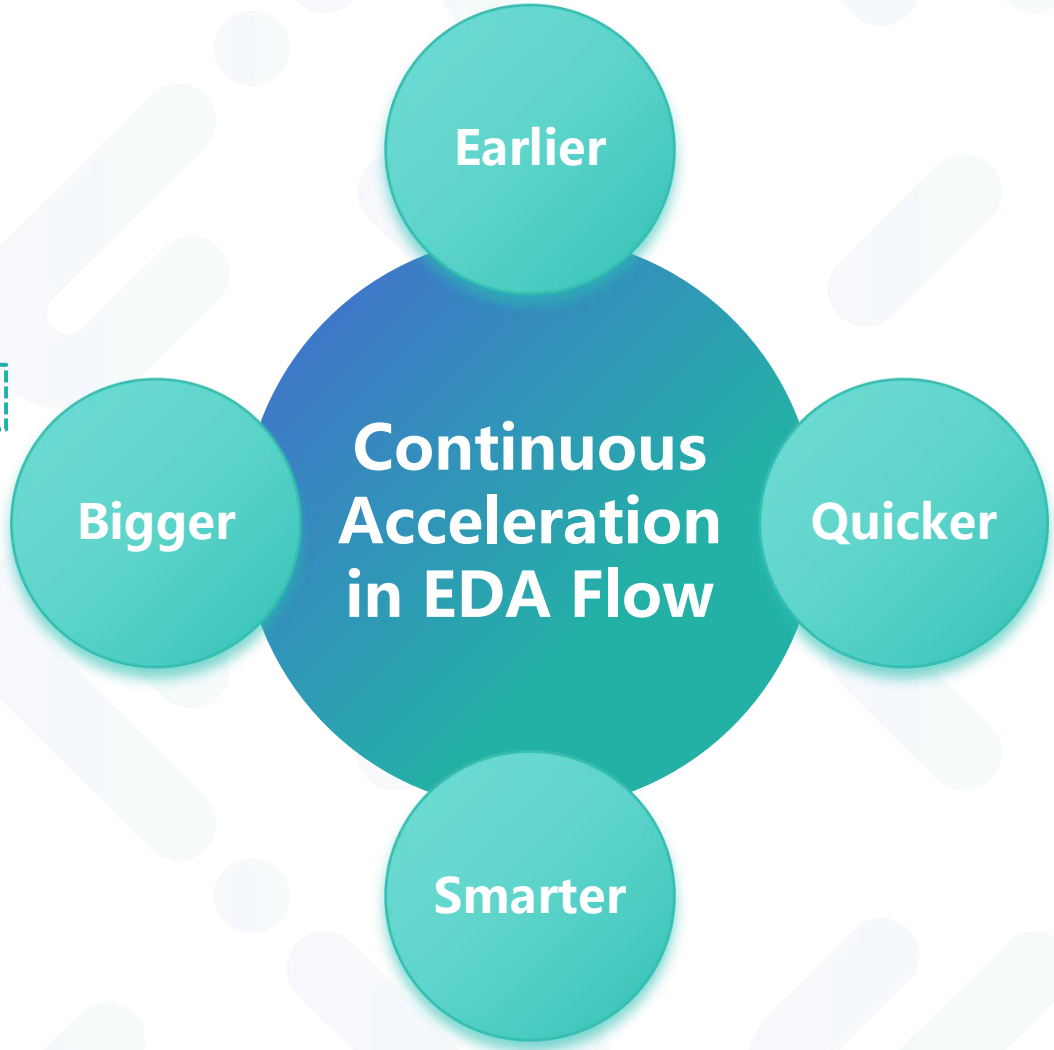

Simulation Tools: Earlier and Continuous in Big System Design Flow

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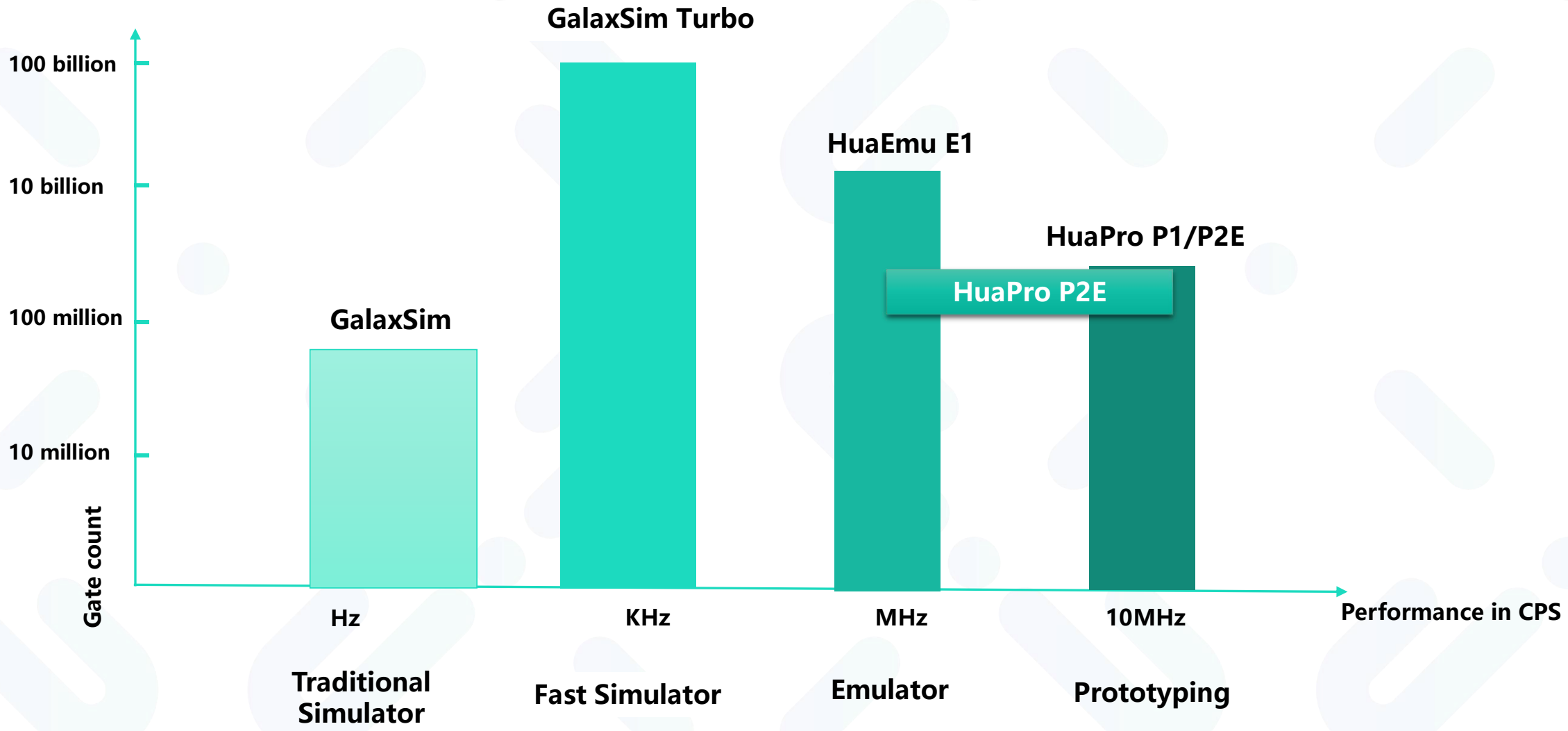
X-EPIC System Level VerificDation Solutions



System level simulation with GalaxSim Turbo for 20 billion GPU design

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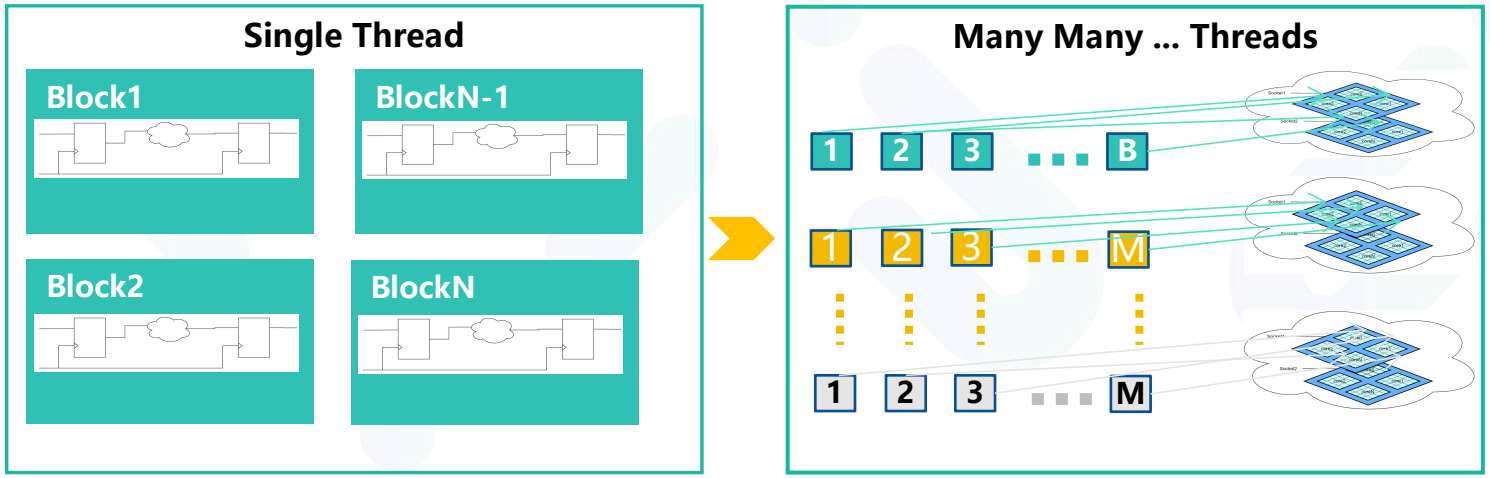
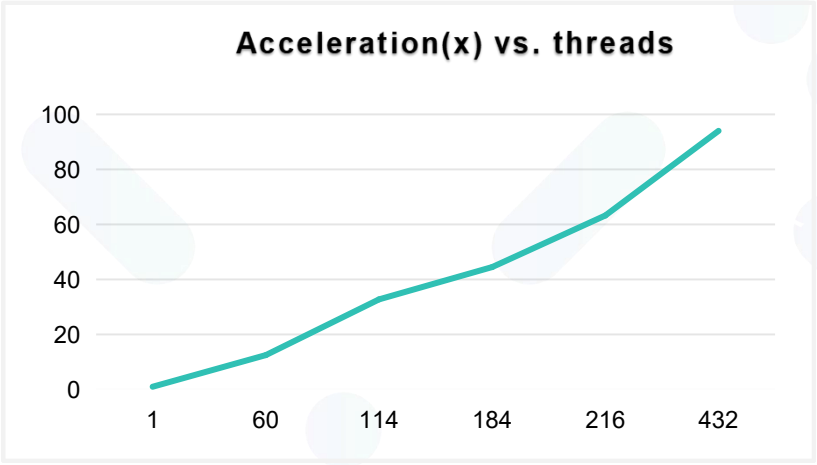
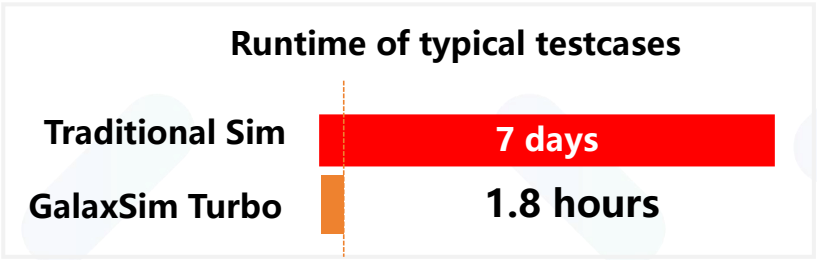
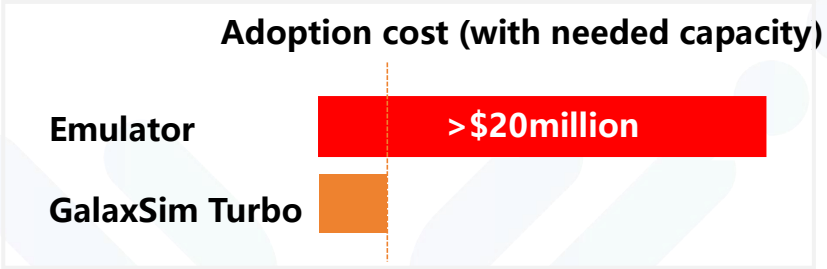


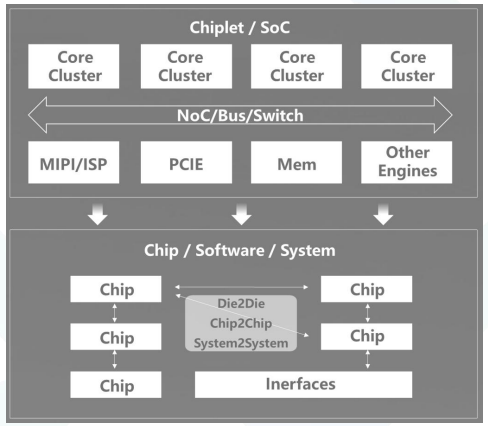
GalaxSim Turbo successfully to the large multi-core GPU design (10’s of billions of gates), Obtaining nearly 100x acceleration ratio, saving over 95% of costs







HuaEmu E1: Bigger Emulator for 10 Billion Level SoC to Chiplets



Super Capacity

- **Design for big designs** – more than 15 billion gates design size
- **High emulation memory** – up to 24TB in one system
- **Flexible adoption**– from single board to multi cabinets
- **Fine-grained multitask** – up to 128 tasks in one system
- **Flexible task relocation**– unique symmetric architecture
- **High utility rate** – cloud-native management system

Powerful Debugging

- **Reduce Recompilation** – full vision
- **Long time tracing** – unlimited depth dumping
- **Locate the bug** – accurate programmable rigger
- **Reproduce the bug** – emulation record/replay
- **System Debug** - context save/restore
- **Automatic Debug** – trigger calling debug command

High Performance

- **High efficiency implementation** – automatic and quick compilation
- **Accelerated P&R process** – unique symmetric architecture
- **High performance** – dedicate optical switching protocol for low latency
- **Low impact debugging** – high speed signal dumping

HuaPro P2E: Innovative Dual-mode Hardware Verification

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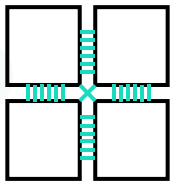
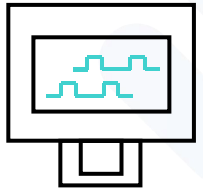
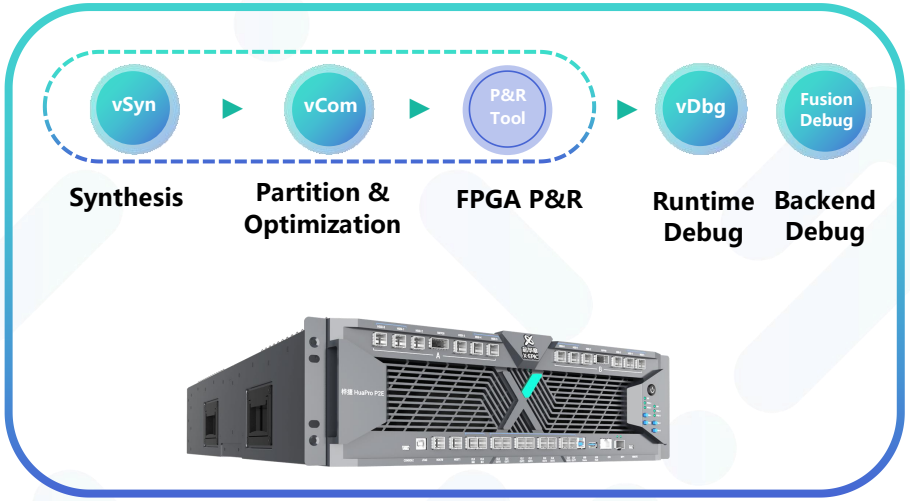
Prototyping Mode

Emulation Mode







Customer A – Prototyping Mode

Size:
- up to 20 FPGA chips

Performance:
- 1 FPGA project - 20MHz
- 20 FPGA project - 10MHz

Prototyping flow bring up time
- Prepare FPGA version: 1 week
- vCom partition iterations: 2 weeks
- PR iterations: 2 weeks
- Performance tuning : 2 weeks

Customer B - Emulation Mode

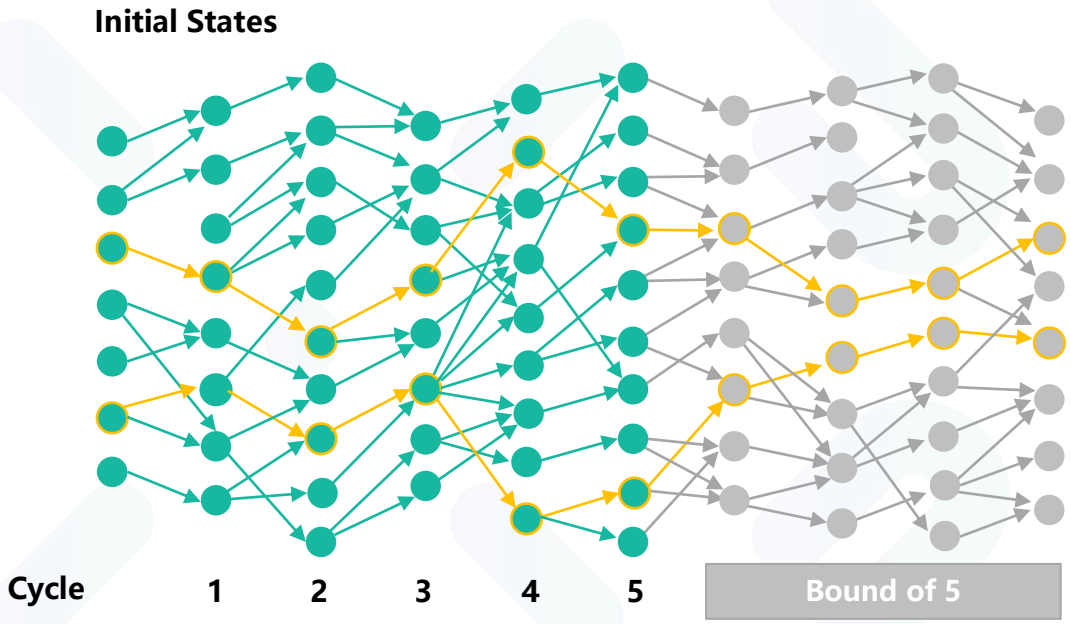
Performance: 6 FPGA，3-4MHz

Emu flow bring up time: 2.5 weeks

Solution: virtual models

Debug: Full vision, Accurate Triggers, etc.

Smarter Verification: More Computing for Less Analysis



Simulation: enumerative method

Formal: Equivalent to an exhaustive approach

$$(x+1)^2 = x^2 + 2x + 1$$

X	$(X+1)^2$	X^2+2X+1
0	1	1
1	4	4
2	9	9
...	...	...

1	$(X+1)^2=(X+1)(X+1)$
2	(X+1)(X+1)=(X+1)X+(X+1)1
3	(X+1)1=X+1
4	(X+1)X=XX+1X
5	$XX=X^2$
...	....

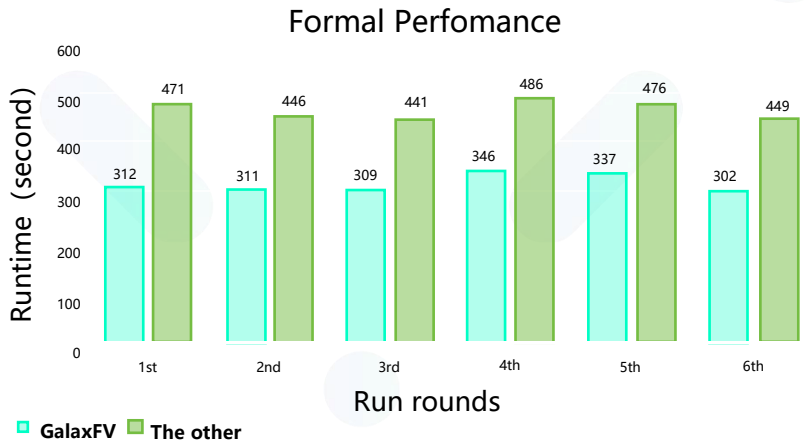
Simulation:
Provides stimulus comparison output

Formal:
Solve for all statesMathematical solving through the solver

Solvers

GalaxFV Showing Competitive Advantage in Multiple Projects

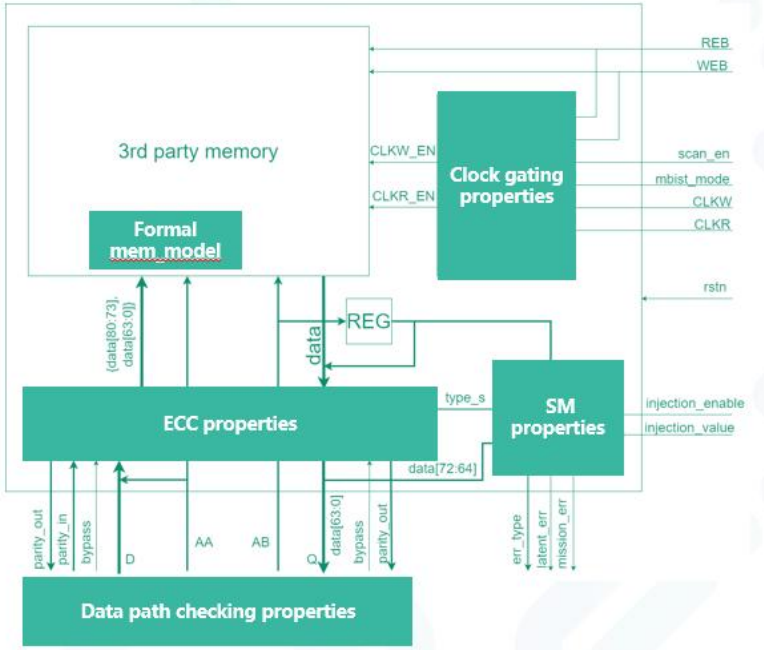
Project 1: FIFO module in a GPGPU chip



1.3x faster
than Tool A
for all properties

ISO 26262
AEC-Q100
Certified

Project 2: Mem Ctrl module in an intelligent driving chip



Property proving time

Tool A	
GalaxFV	3x faster

Project 3: Datapath with large data bit-width in an ADAS chip

Property proving time of 128 properties

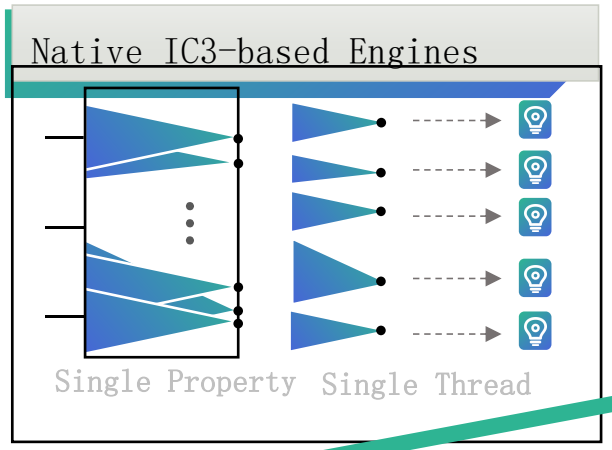
Tool B	30 hours still unsolved
GalaxFV	2 hours solved

- **Addressed Challenges:** Large design space, Complicated algorithm

- **Application Library:** Mem model, error-injection model

* Tool A and Tool B are Main Stream FV tools

How Fast Can We Do Formal UMC?



FASTEST

FASTER

FAST

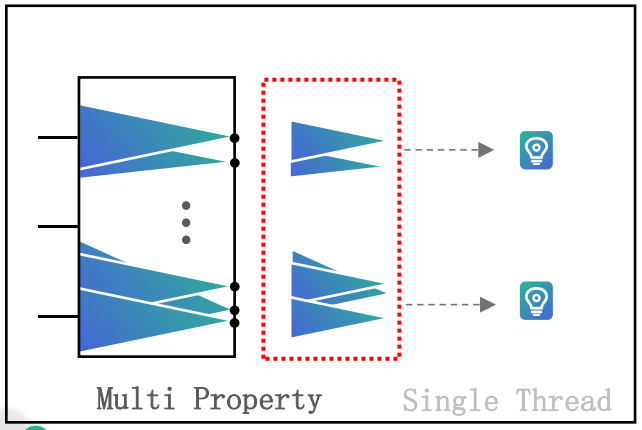
SLOW

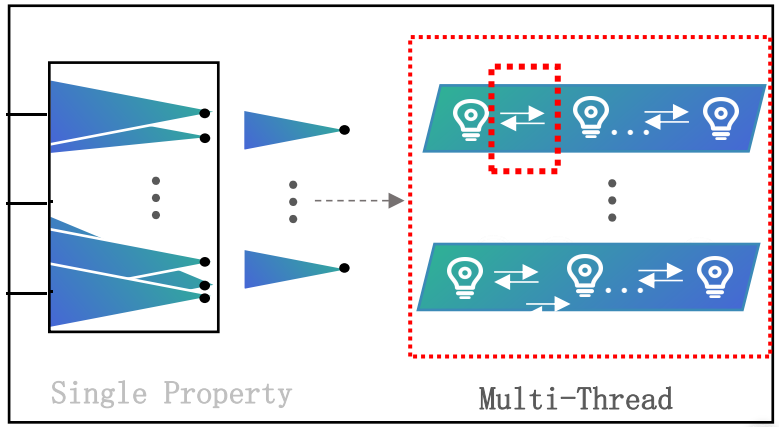
Property Clustering, P-PDR & D-PDR
are orthogonal factors
2 x (10~400) x (5-10) = 100sX Speedup

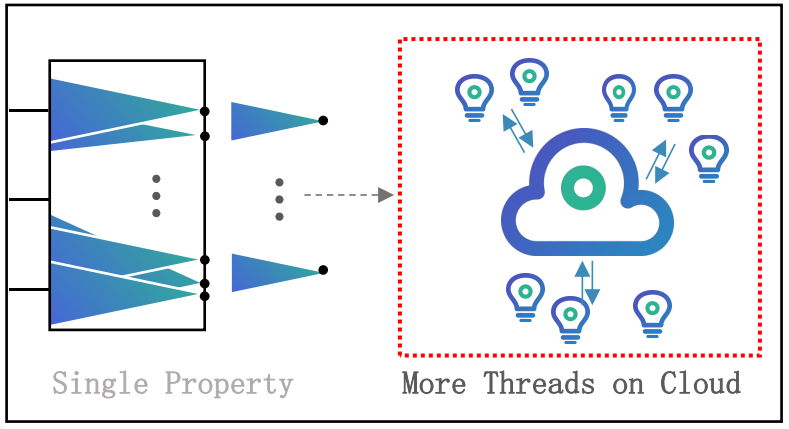
Original speed | 2X speedup factor | 10X to 400X speedup factor | 5X to 10X speedup factor

: Single property

: IC3-based Engine







COI-Native Property Clustering → P(arallel) PDR and Lemma-Sharing → D(istributed)-PDR

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Galax Formal: Smarter Verification Methods with Quicker Engine

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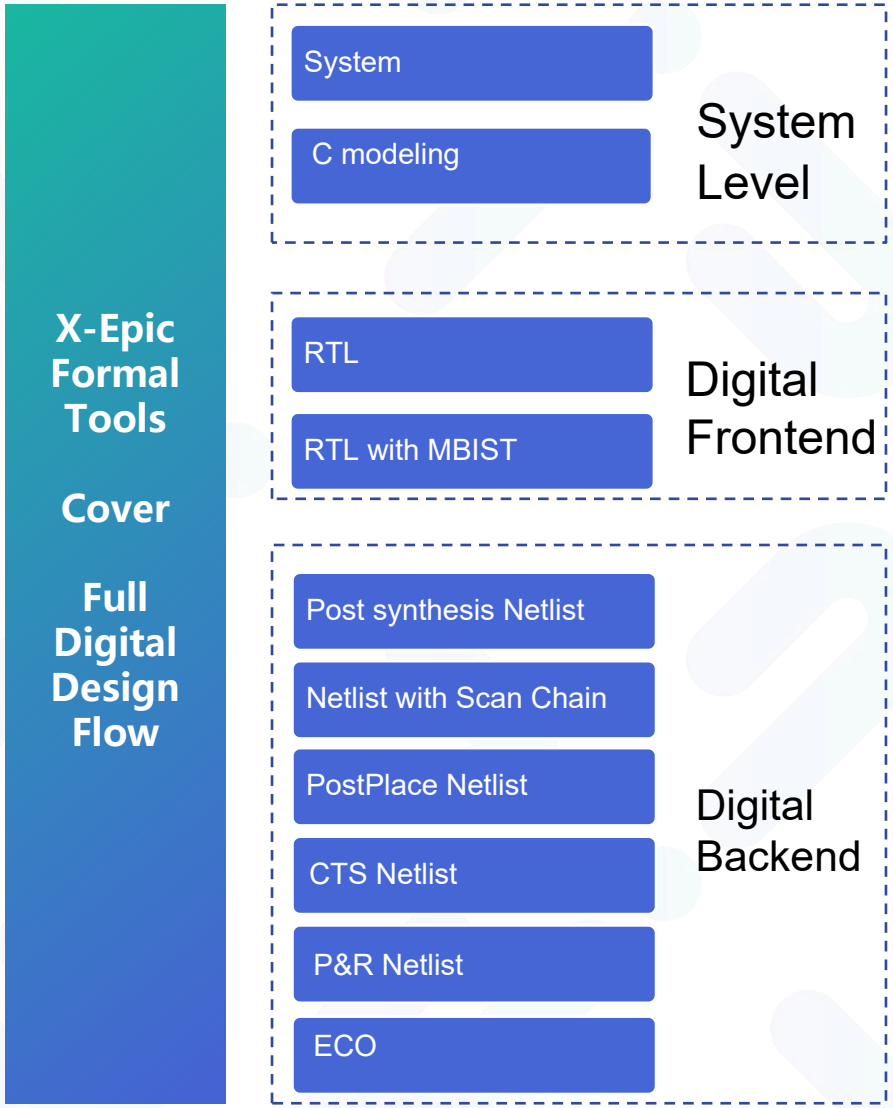


HEC
High Level Equivalence Checking

C/C++ model VS RTL checking, often used in data path algorithm design flow

Model Checking
Model Properties Proving

Static formal proving based on properties, for complete design function verification

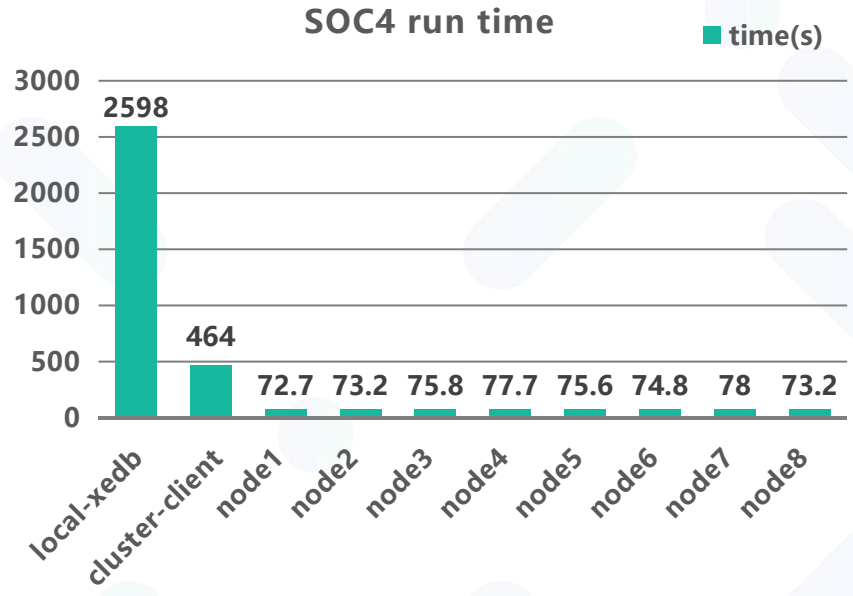
SEC
Sequential Equivalence Checking

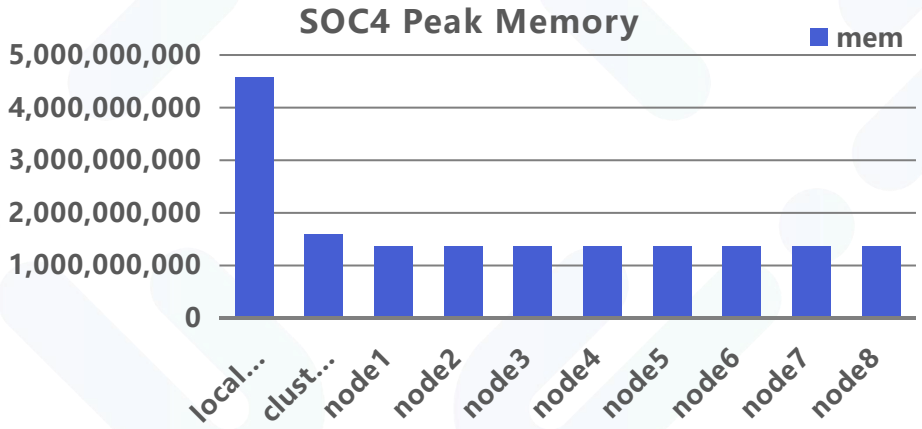
Exhaustive equivalency checking for circuits with state transitions and outputs

LEC
Logic Equivalence Checking

Check different representations of a combinational circuit are functionally equivalent

XEDB: Quicker Database to Improve Efficiency





Case Name	Number of signals	Number of vc
SOC4	10million	10,000 million

Case Name		Run time	Memory
SOC4	local xedb	43m18.476s	3.95G
	cluster-xedb	7m44.946s	1.59G
	xedb-node	72s ~ 78s	1.35G

Prove distributed XEDB write times compared to XEDB Reduced by more than

5X

Cloud Native EDA: Unlimited Computing for 100x Accelerating

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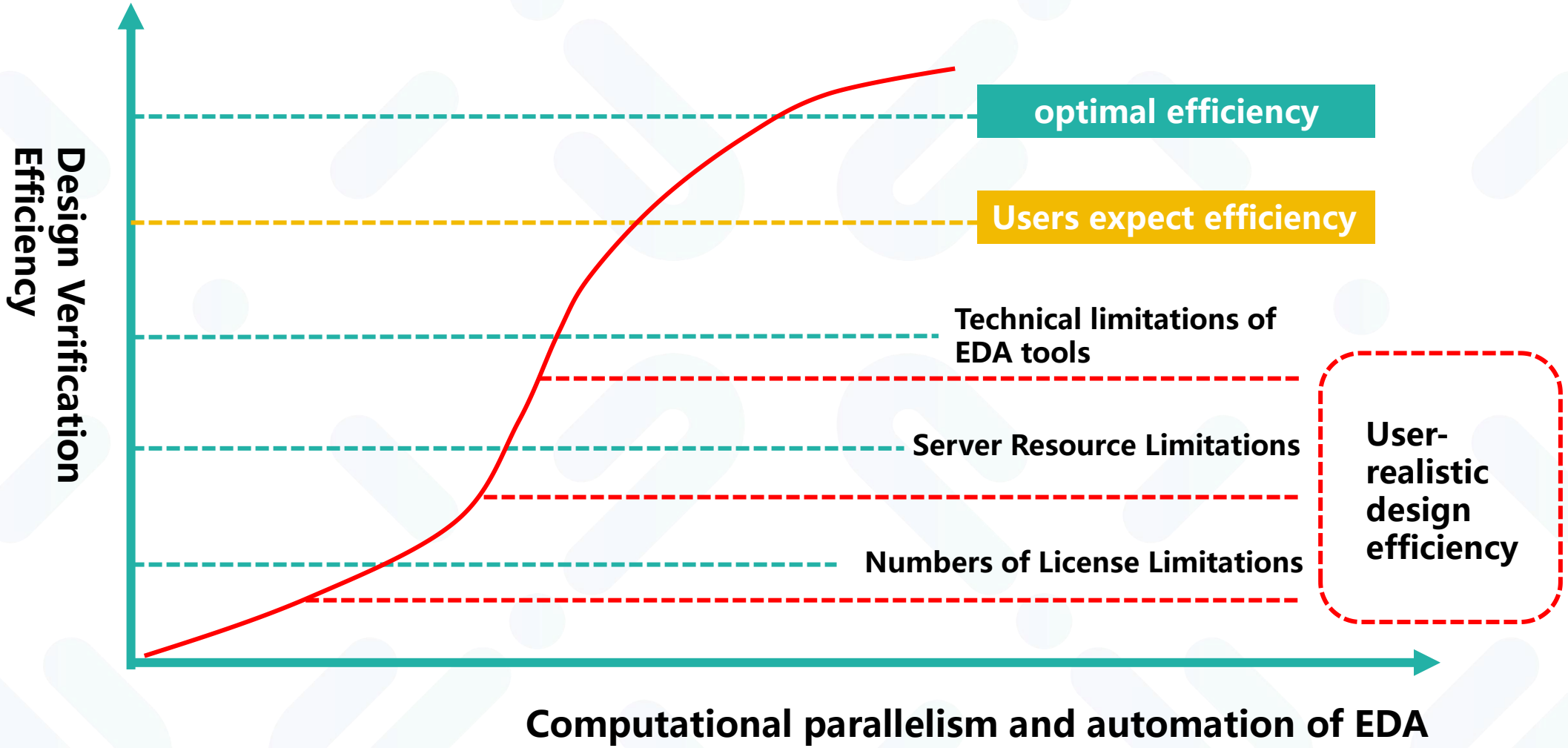

Debugging with Data Driven methods

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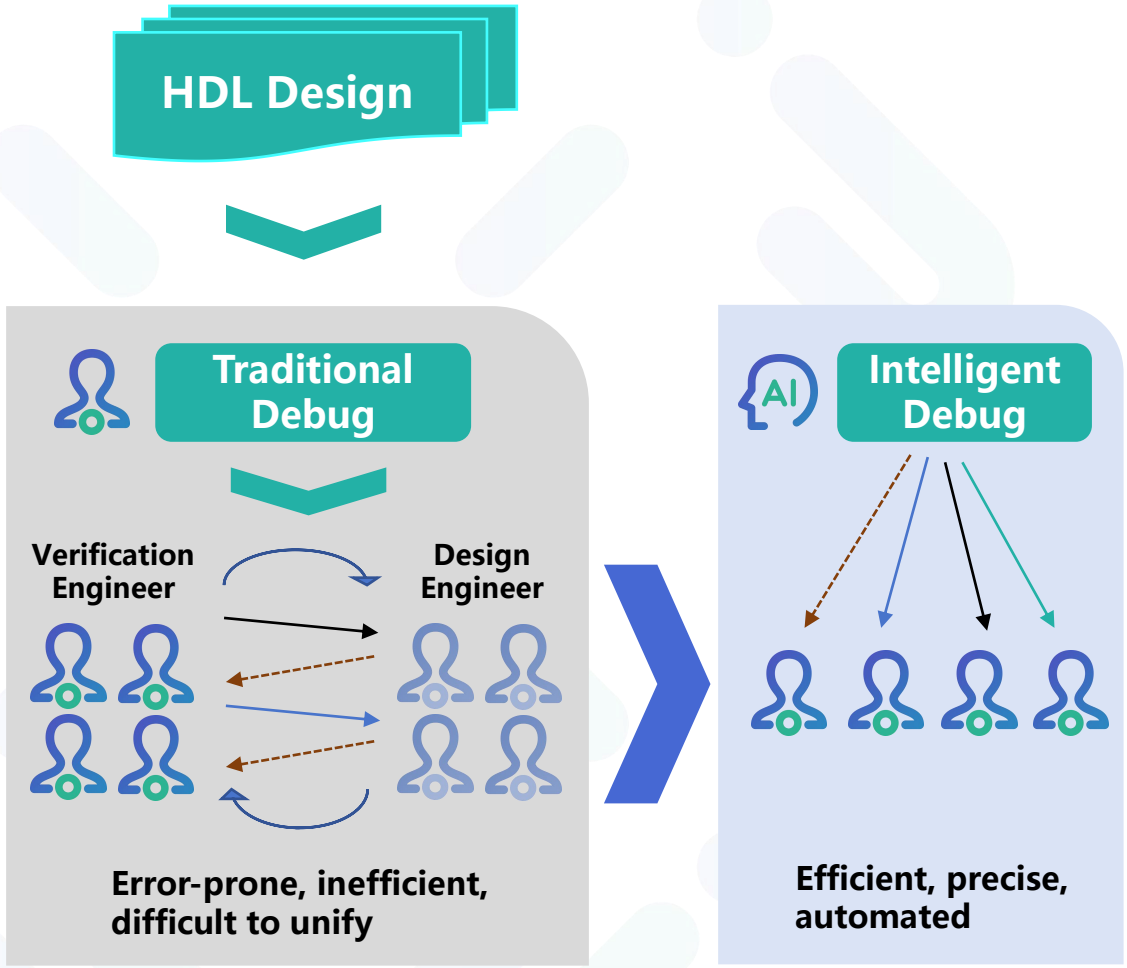


Use NLP to improve adaptability

User prompt

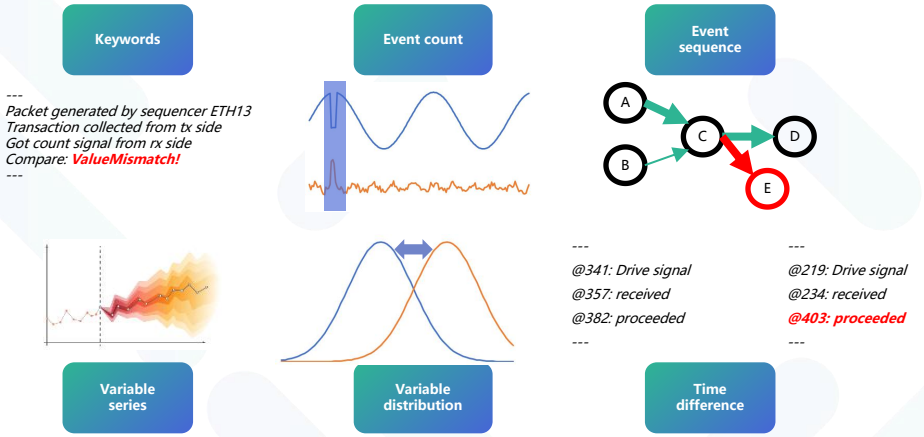
a. UVM_INFO ...@...: data transmitted via Ethernet

b. UVM_INFO ...@...: data sent by Ethernet

Q: Are they from the same log event?

AI **Yes, they are the same event**

Rich failure-type mining models



XEPIC provides platform and tools for Agile Design Verification

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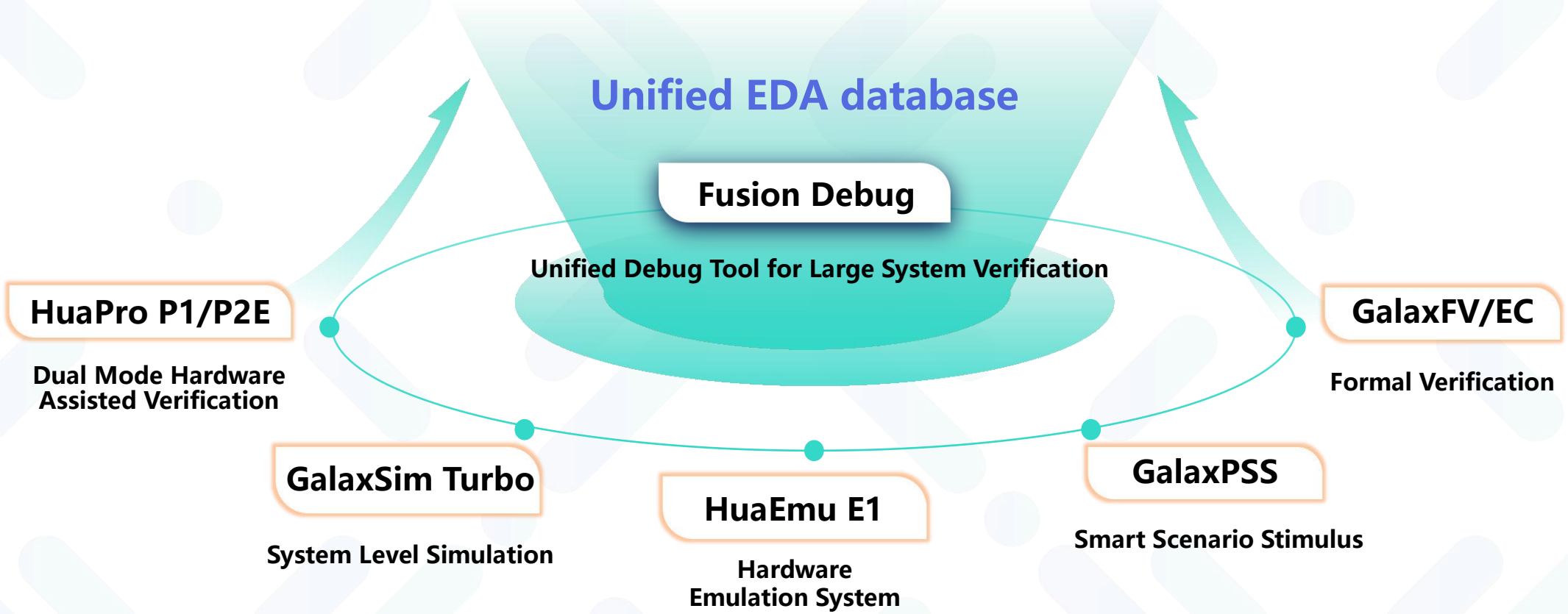
Continuous Acceleration for Agile System Verification



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Accelerating System Verification