

AI-Driven Verification

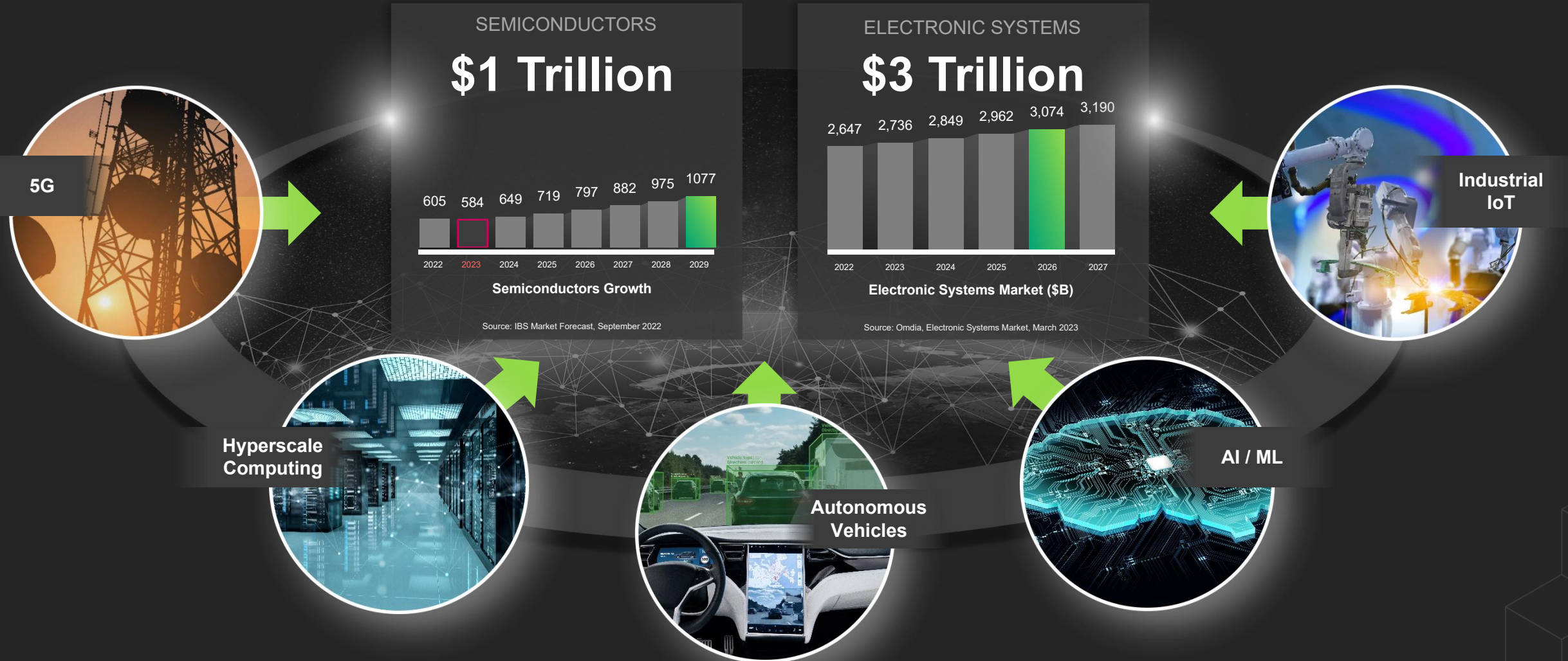
Leveraging AI to Achieve the Next Leap in Productivity

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VP Product Engineering, Systems and Verification Group

 cadence®

Five Generational Trends, All Anchored Around Compute



Productivity Challenge in Chip and System Design

Complexity Is
Increasing

100X

Over the
Next Decade

Source: Cadence analysis

More Annual Design
Starts

4X

Over the
Next Decade

(<=10nm)

Source: IBS Global Semiconductor Industry Service Report: Design Activities and Strategic Implications, July 2022
Source: Cadence analysis

Not Enough
Engineers

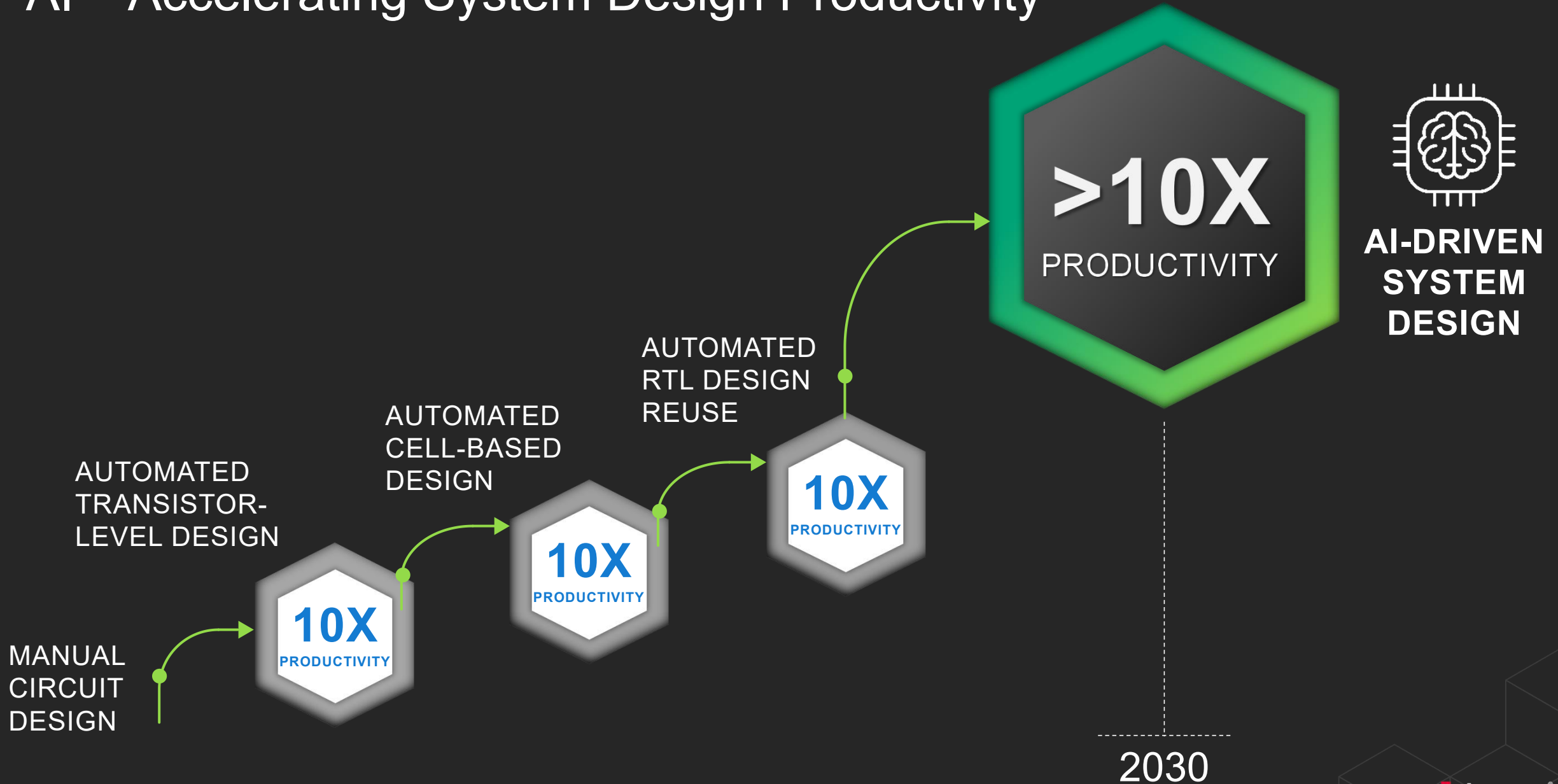
Semiconductor Engineering

**Engineering Talent Shortage Now
Top Risk Factor**

FEBRUARY 25TH, 2019 - BY: [MARK LAPEDUS](#)

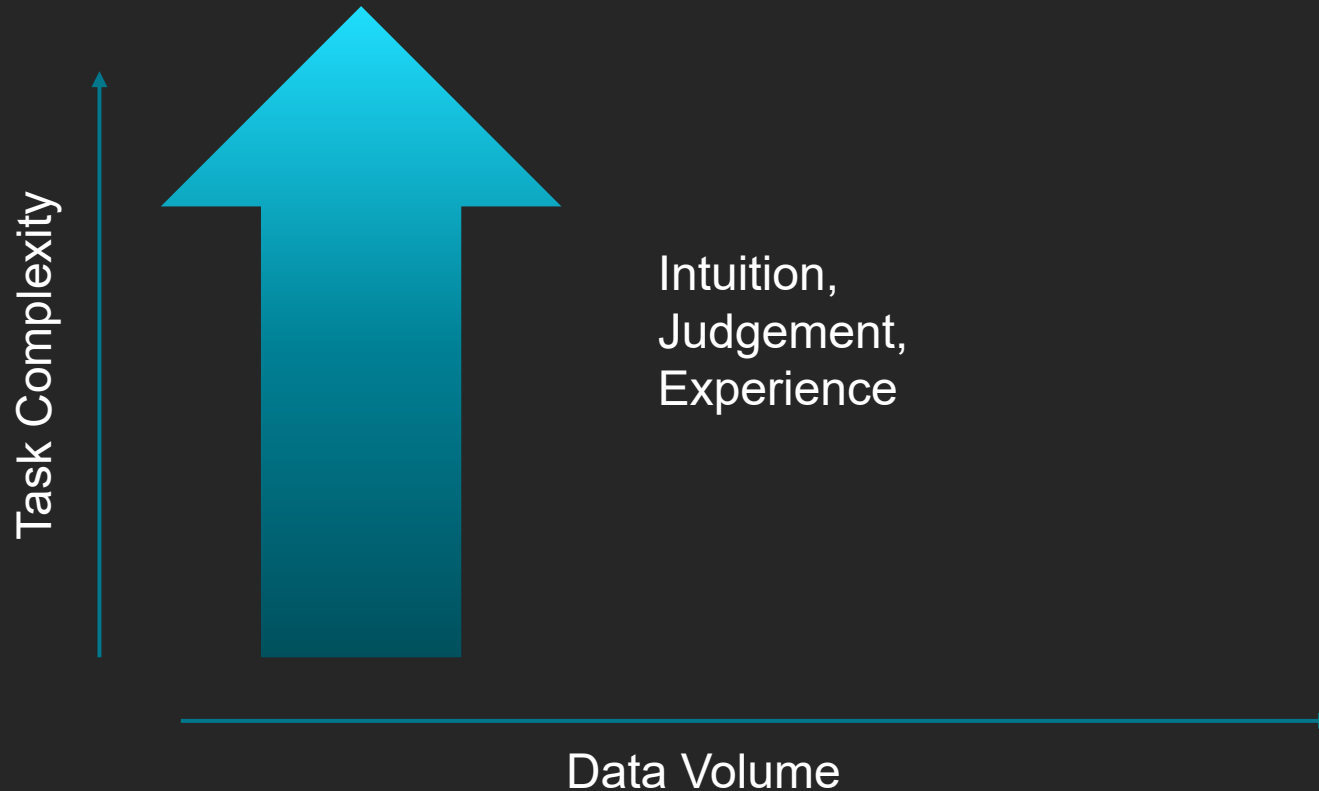
Source: <https://semiengineering.com/engineering-talent-shortage-now-top-risk-factor/>

AI – Accelerating System Design Productivity



Power of the Human

Human engineer: solve complex problems and be creative

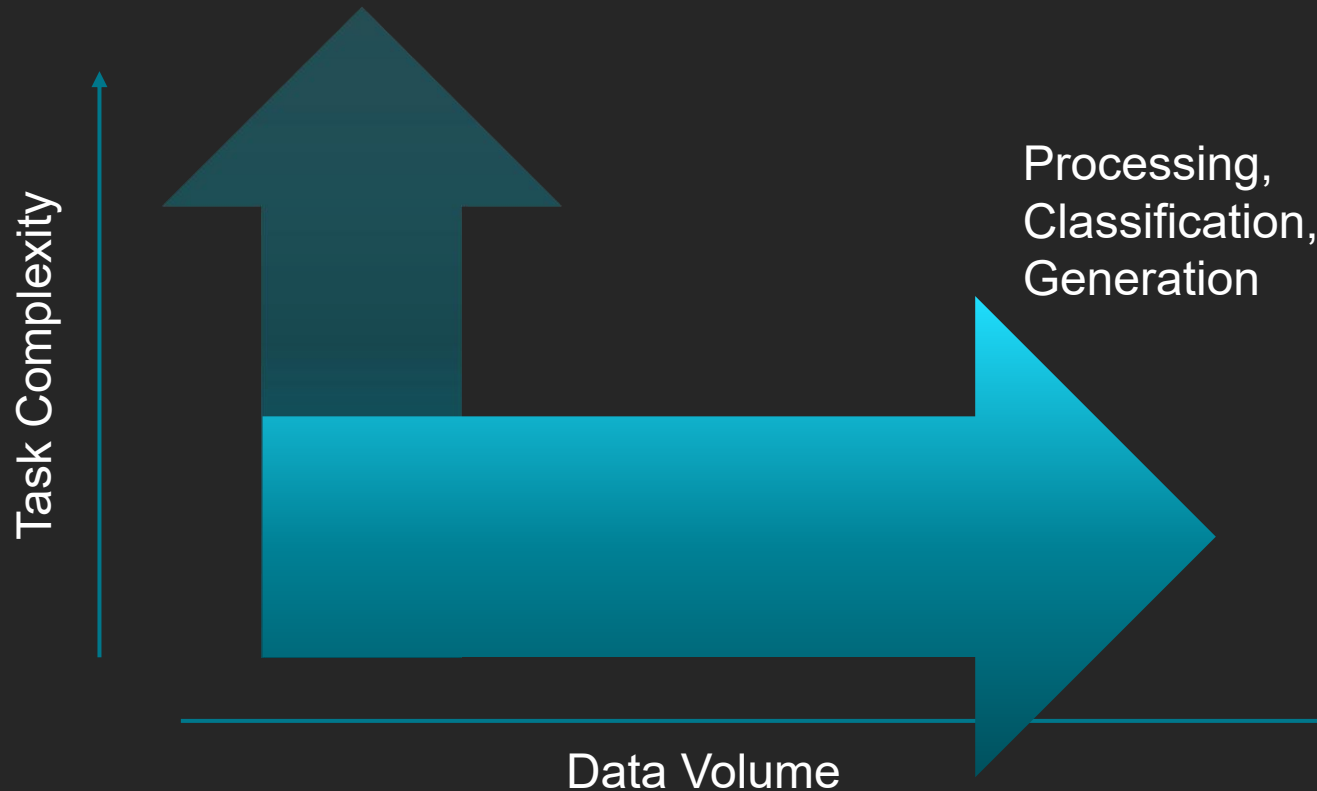


- Design algorithms
- Innovate new architectures
- Think outside the box

Power of AI Algorithms

Human limitation: serial data processing

AI strength: insights from parallel processing big data



- Chat bots
- Speech from text
- Image from text
- Recommending ads
- ...

Power of AI-Driven *Solutions*

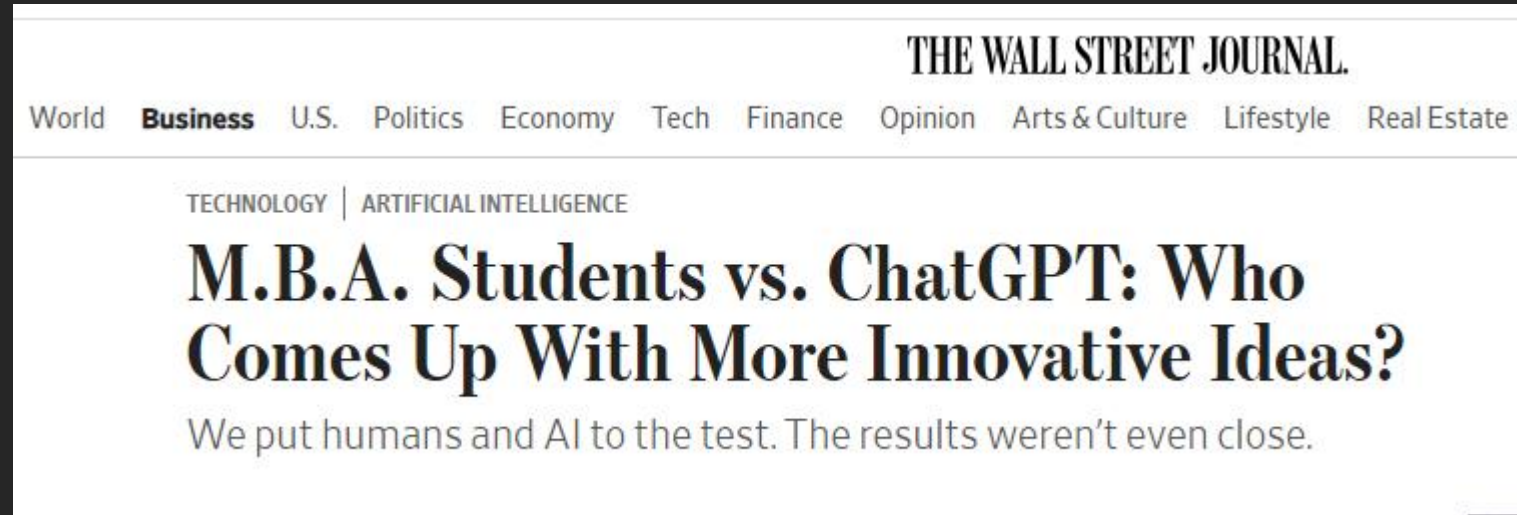
Accelerate the human in the loop



Human in the Loop AI Solutions – Pilot & Co-Pilot

“...rather than thinking about a competition between humans and machines, we should find a way in which the two work together”

Terwiesch & Ulrich – wsj.com



Challenge – Generate 200 “New Business” ideas : AI (ChatGPT) - ~1h;
Humans (Wharton MBA Students) – Days

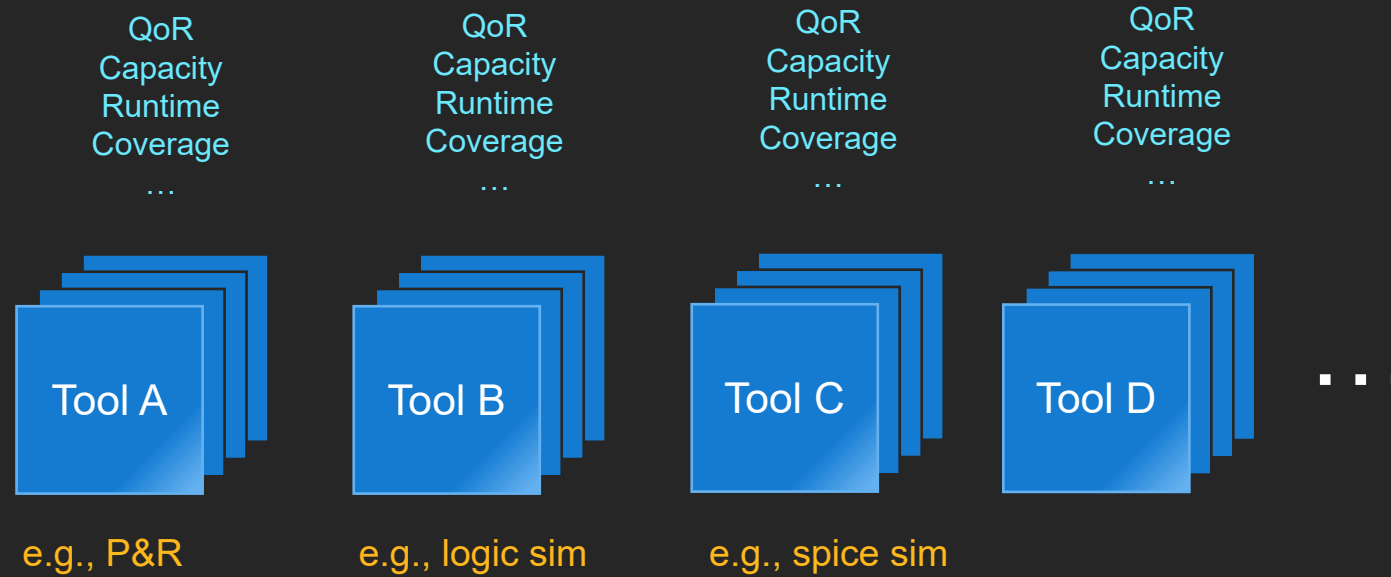
Human in the loop AI – Pilot & Co-Pilot

Human (Pilot) – Identify the problem.

AI (Co-pilot) – Report what is known about the problem.

Human + AI – Iterate on unique and creative solutions to the problem.

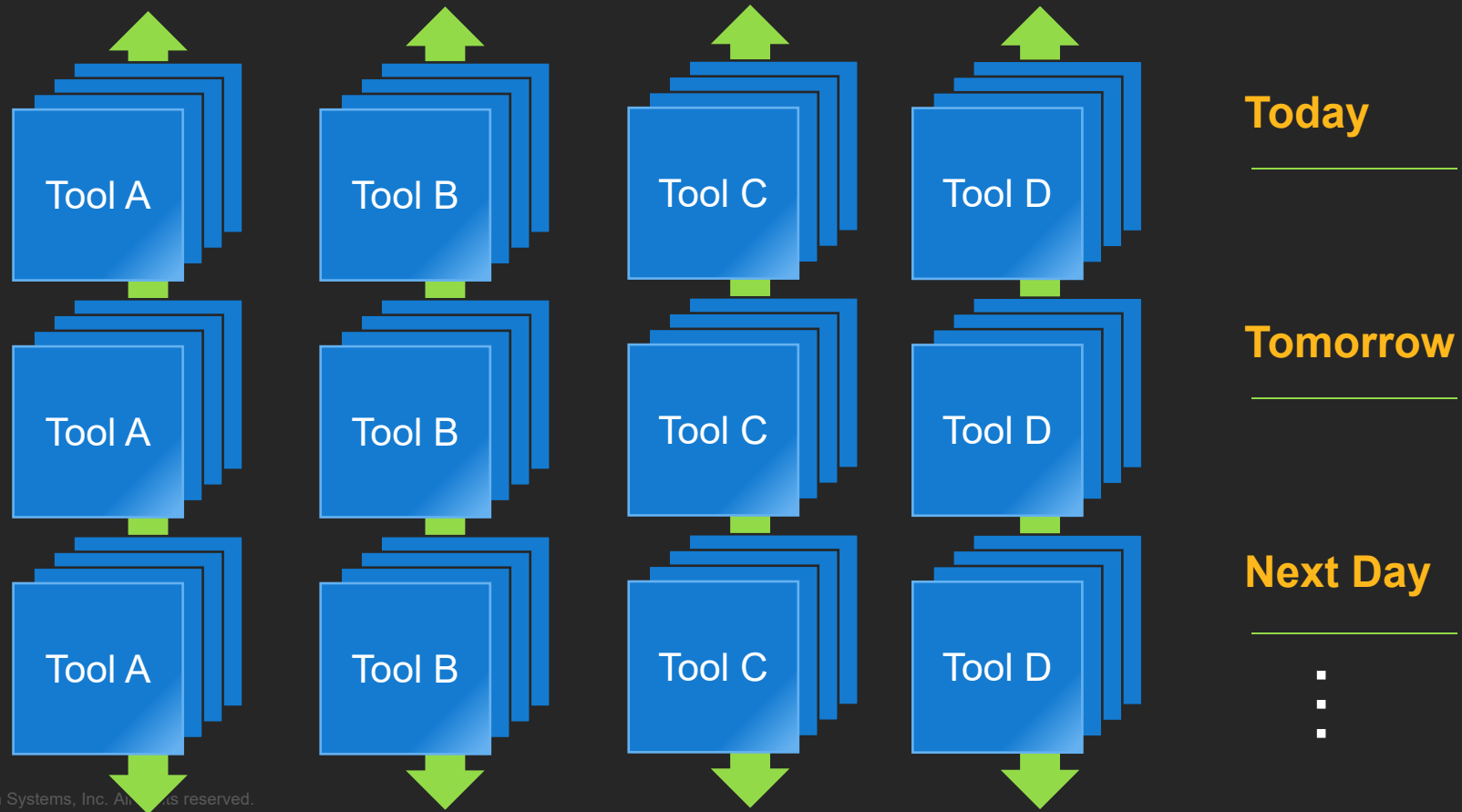
Traditional EDA



User Perspective

Meet PPA Goals
Meet Coverage Goals

...



Next Generation AI-Driven EDA



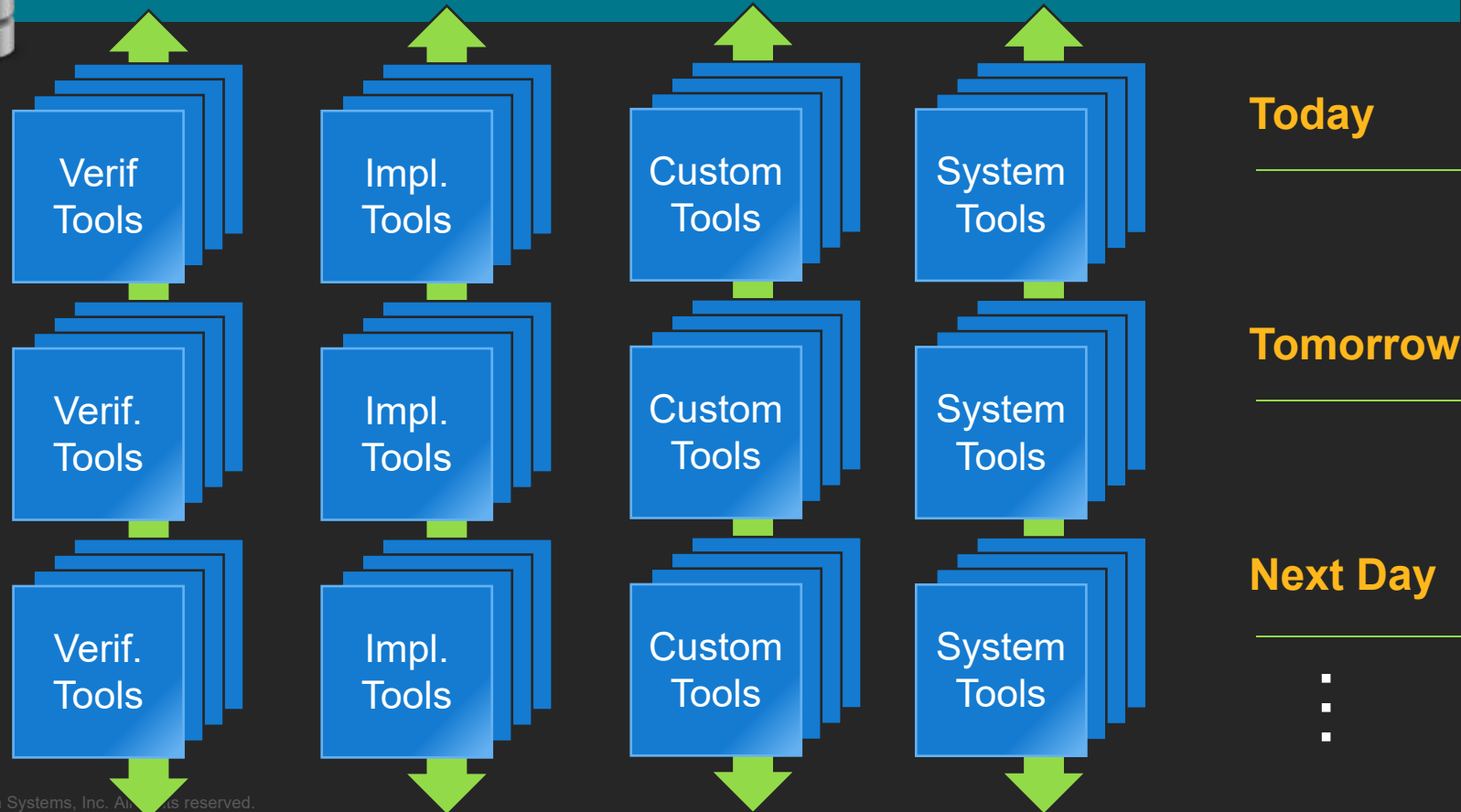
AI-Driven Design and Verification

Multi-engine multi-run learning and optimization

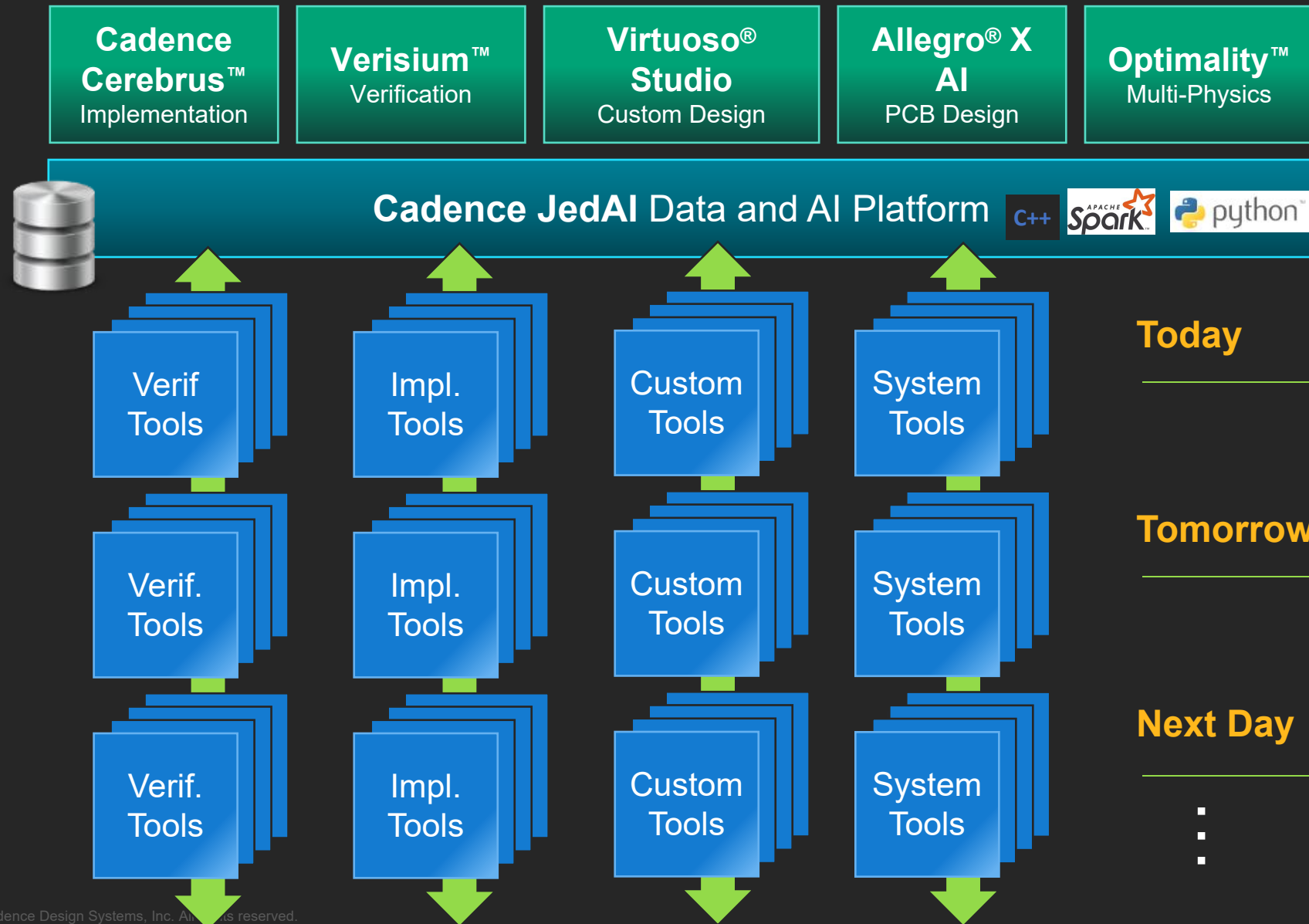
*Best PPA
Highest coverage
Fastest time-to-market*



Big Data Platform



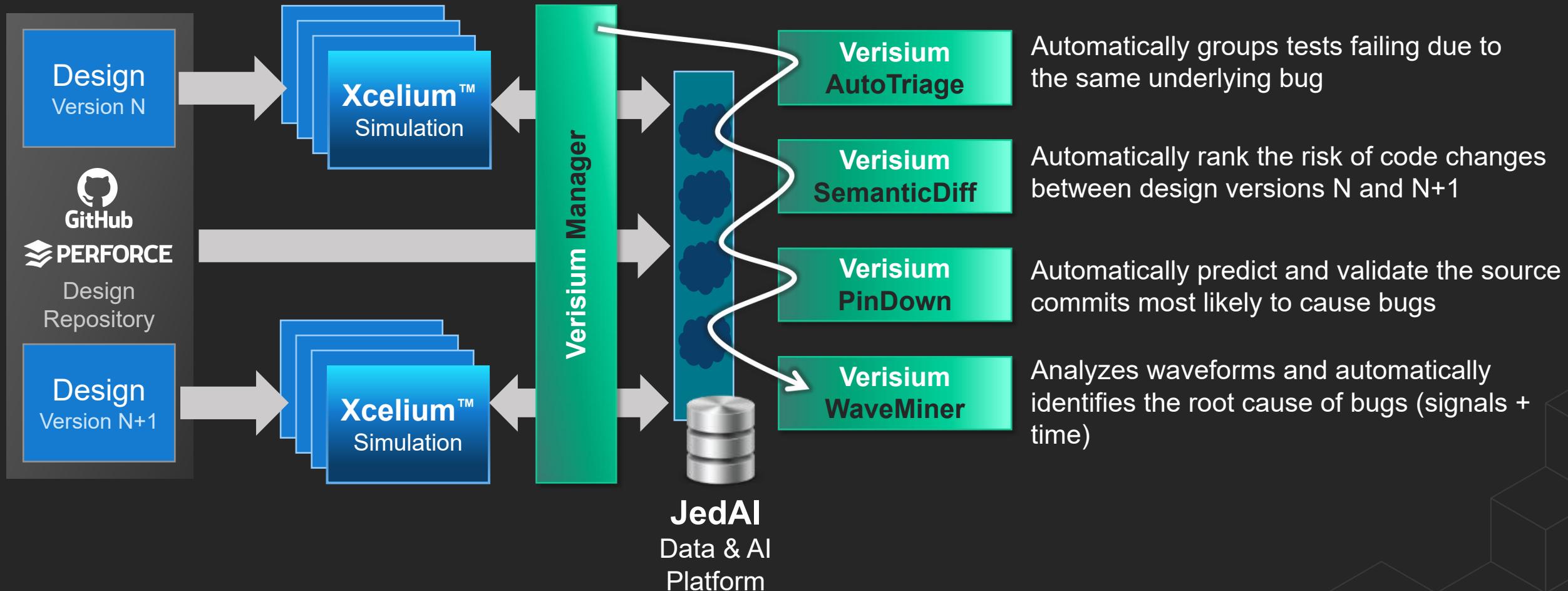
Cadence AI-Driven Transformation



Next-Generation AI-Driven Verification Workflow

Cadence Verisium™

AI-driven submission of
tests to compute farm



AI Driven Workflow: 3x – 60x Productivity Gain

Verisium™ Results

30X

Faster Waveform Analysis
Memory Controller IP

3.3X

Reduction Failure Triage Time
Block and System-Level Regressions

6X

Total Debug Effort Improvement
Automotive SoC

60X

Less Effort for Design Change Analysis
>1B Gate Mobile SoC

10X

Productivity End to End SoC Debug
Mobile SoC

4X

Faster Identification of Buggy Source
Interface IP

4X

Better TaT for Bug Fixes
CPU Core IP

20X

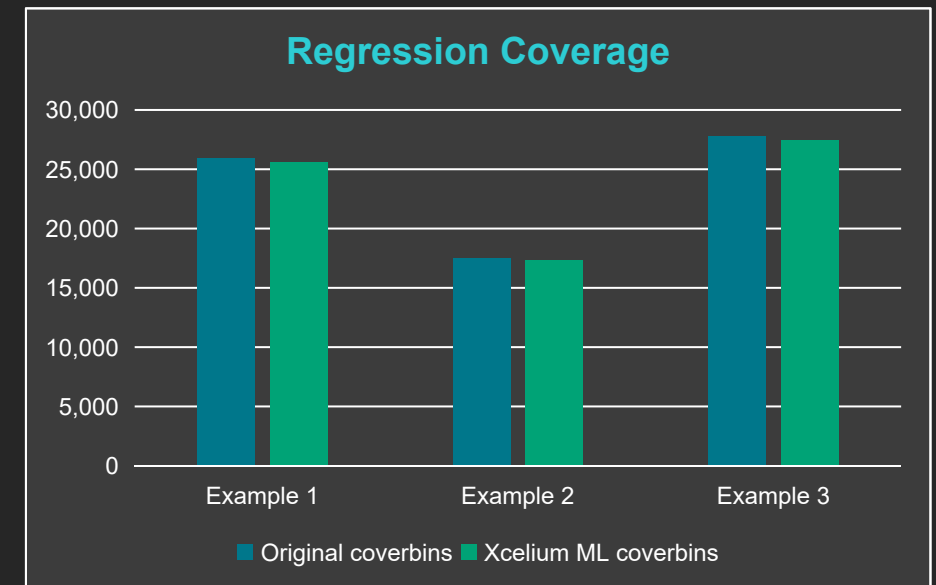
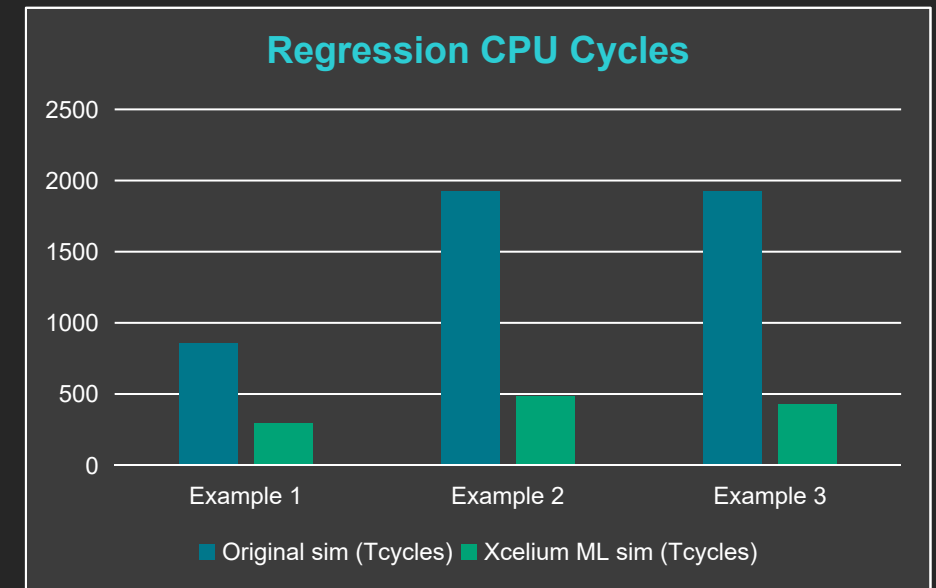
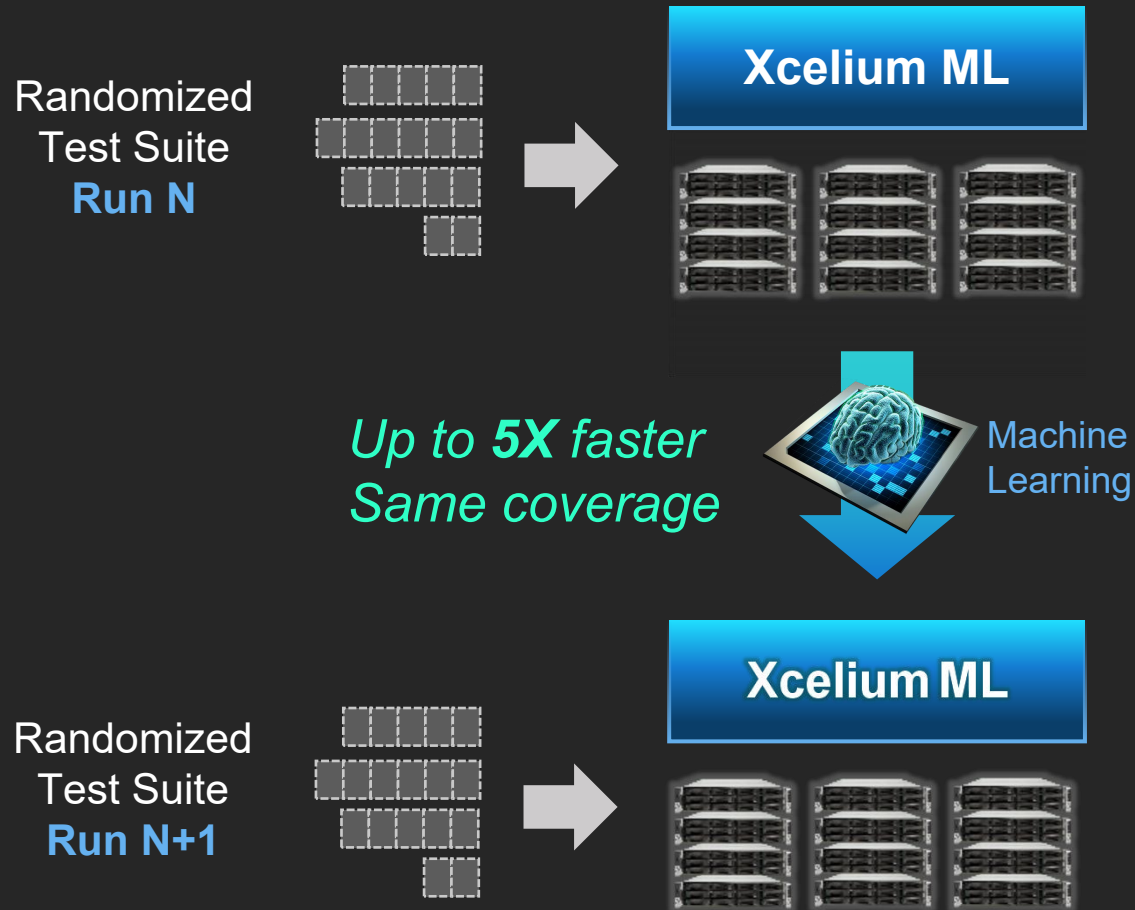
Faster Verification of Changed RTL
RISC-V CPU

8X

Regression CPU Time Reduction
Image Sensor IC

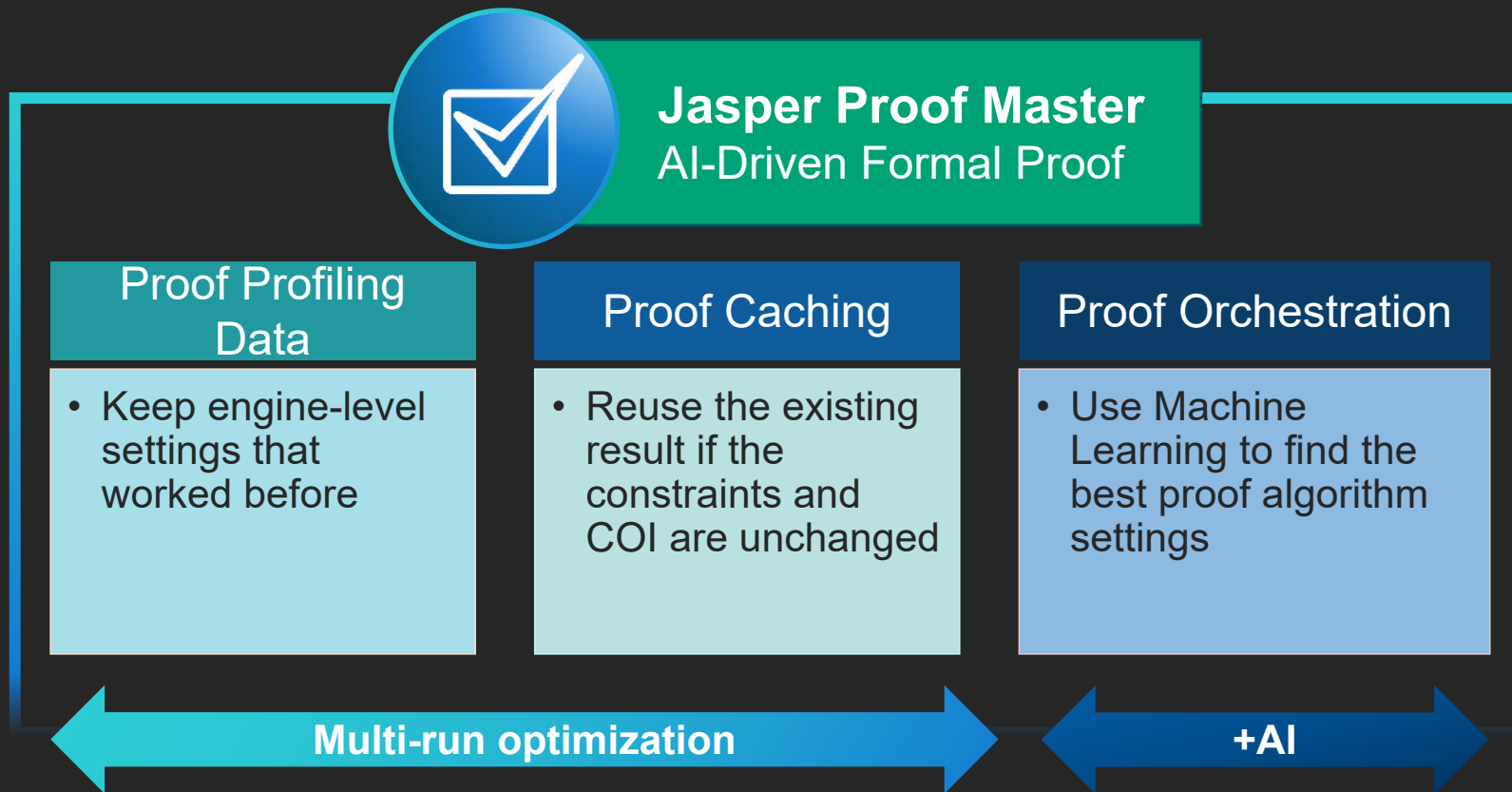
AI-Driven Simulation Performance

Cadence Xcelium™ ML



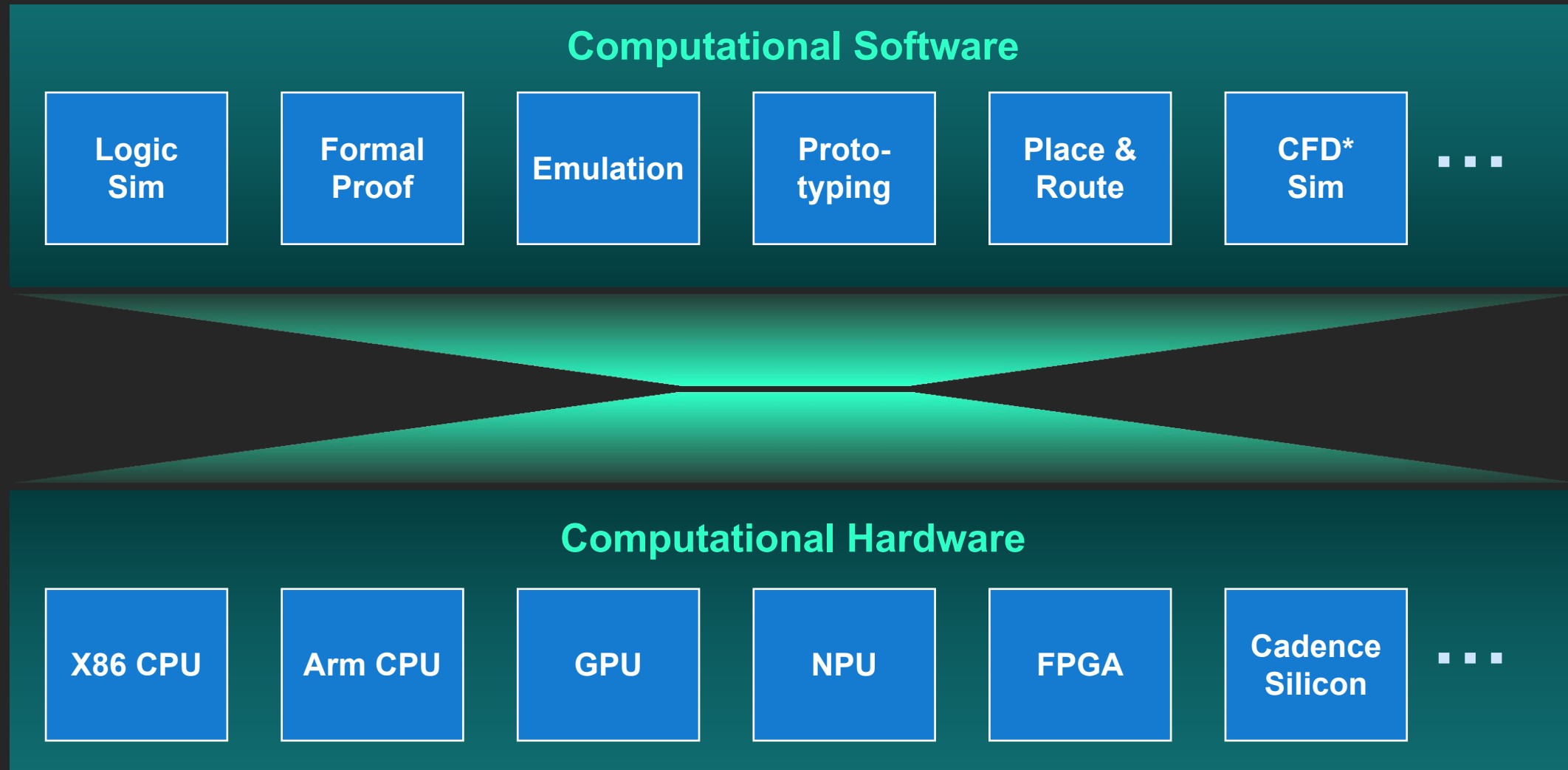
AI-Driven Formal Proof

Cadence Jasper™ Proof Master



Testcase	Baseline	Smart Proof	Gain
A	50%	59%	1.2X
B	69%	69%	1.0X
C	12%	25%	2.1X
D	44%	83%	1.9X
E	57%	94%	1.6X
F	68%	69%	1.0X
Total	53%	71%	1.3X

Domain-Specific Compute in EDA



Domain-Specific Compute for EDA on the Cloud



Cadence Cloud Service

Pop-up ready-to-go full flow
for design and verification

Foundry and IP partner
security certified



Cadence Cloud Passport

Cadence tool licensing
enabled on the cloud

On-Premise Tools



Cloud
Passport



Cadence OnCloud

New SaaS-based
cloud native solutions



Multiphysics Analysis



CFD Simulation



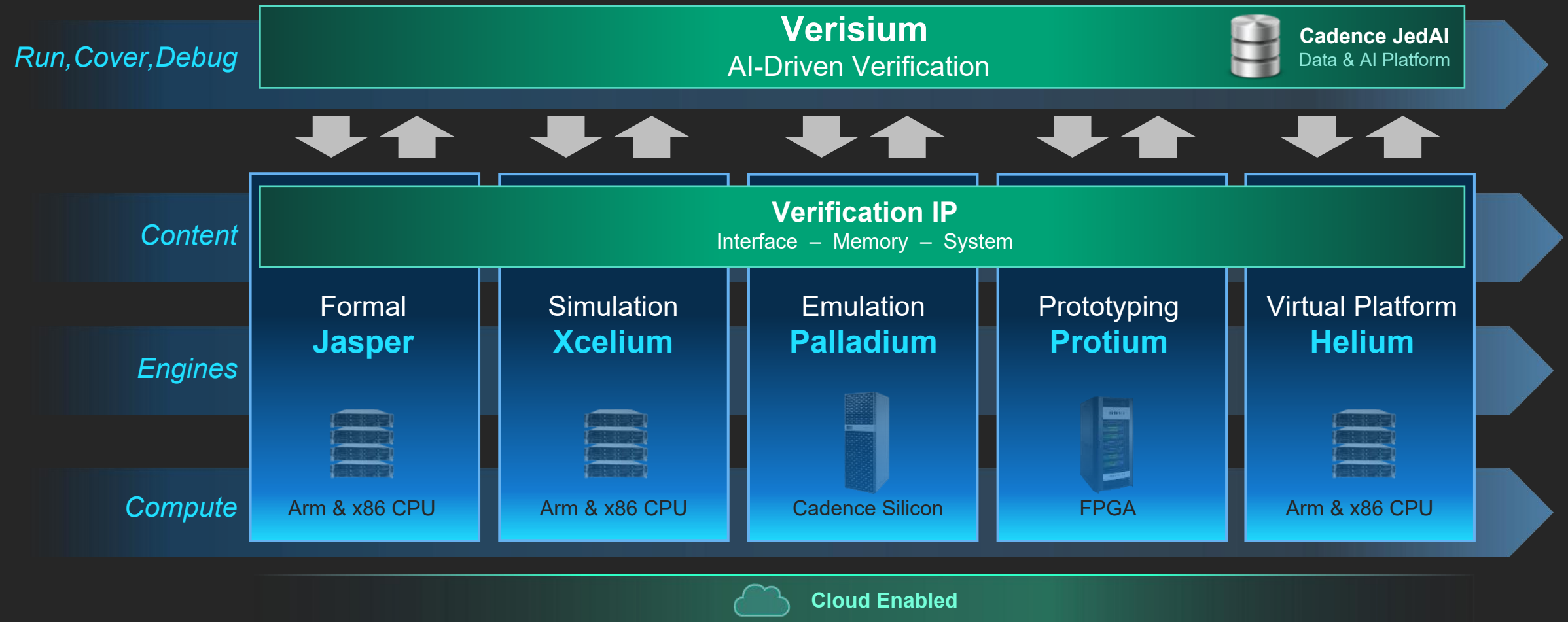
Allegro PCB Design



Palladium
Protium

Next-Generation AI-Driven Verification Full Flow

Cadence Verification Solution



The Cadence logo features the word "cadence" in a white, lowercase, sans-serif font. A small red horizontal bar is positioned above the letter "a". A registered trademark symbol (®) is located to the upper right of the word. The logo is centered on a dark gray background. In the top-left corner, there is a decorative pattern of overlapping hexagons, some of which contain small white triangles pointing towards the center. In the bottom-right corner, there is a pattern of larger, outlined hexagons.

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