Explore the Potential of AI to Accelerate Formal Verification

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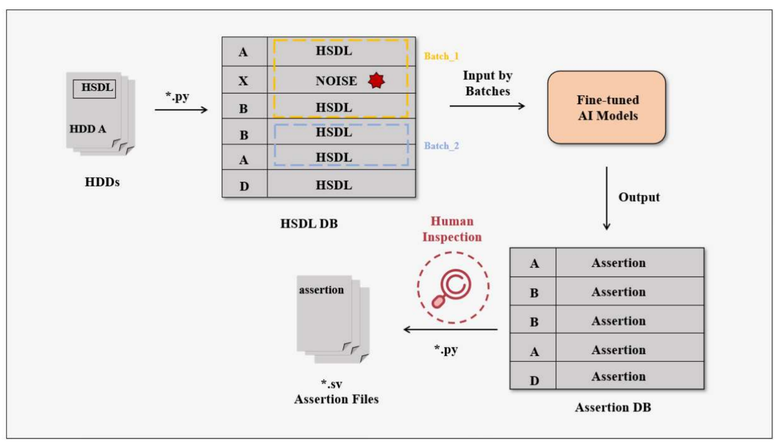
MOTIVATION

Nowadays, the exponentially grown scale of System on Chip (SoC) and the ever-increasing systematic complexity have posed new demands on the efficiency and effectiveness in the entire project life cycle of the circuit design. Thus, it is of great significance to speed up the setting up of testbench and closure of coverage.

Formal property verification (FPV), which utilizes property assertions and does not require the tedious and annoying construction of testbench environment in the first place, thereby boosting the process of verification and facilitating the "left shift" of bug identifying. However, FPV still suffers from certain disadvantages, such as the requirements of substantial computing resources and cumbersome tasks to write considerable assertions as the scale of the design grows, which hinder its practical usage to a certain extent.

PROPOSED METHODS

In this work, we explore the possible application of artificial intelligence (AI) on the formal property assertion generation and demonstrate a promising solution to accelerate the formal verification, and details are illustrated as follow.

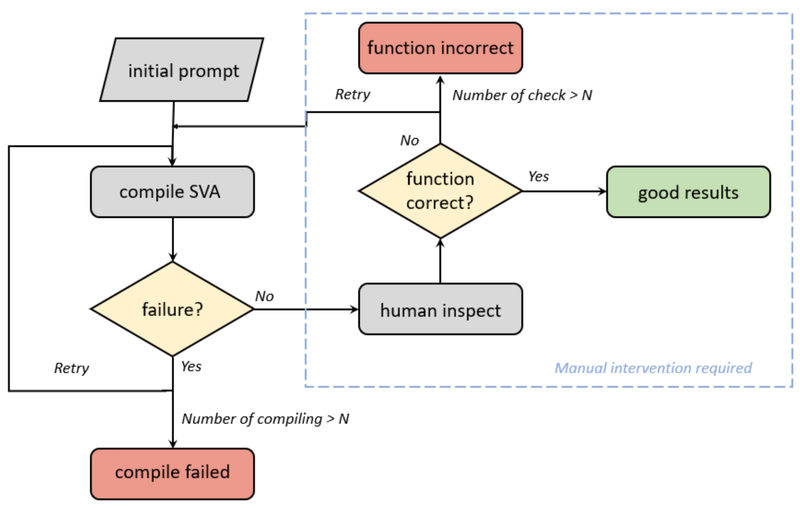


IMPLEMENTATION DETAILS

[Initial Prompt Example]:
We are working on writing the corresponding assertions for an *asynchronous fifo* based on systemVerilog.

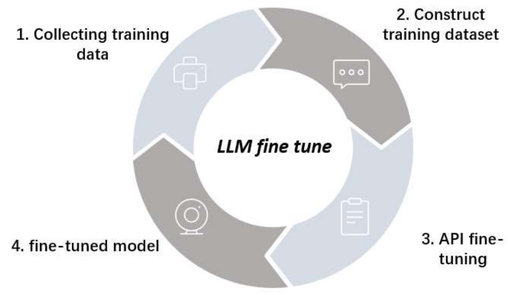
[*Extracted HSDL enrty. e.g.,* the signal data_wr in the design to be tested satisfies the following timing: the *data_wr* signal should not be in the *X/Z* state when the signal *valid_wr* is valid;]

Can you give an appropriate assertion?



IMPLEMENTATION DETAILS

The basic idea of fine-tuning is to take a pre-trained language model that has been trained on a large number of texts and then continue to train it on a small scale of task-specific texts. In the process, the weight coefficients of the pre-trained model are updated to better fit the task. In the work, we use the api approach provided by OpenAI for fine tuning.



JSONL data for fine tuning

- ✓ {"prompt": "<Input query prompt>", "completion": "<Assertions that are expected>"}
- ✓ Example: {"prompt": "<HSDL prompt>", "completion": "<SVA>"}

RESULTS

Tests were performed on chatgpt-3.5, chatgpt-4 and LLM before and after fine tune. Although the inherent language generation capability of the Davinci model itself is not as good as chatgpt4, the Davinci model, after fine-tuning, has a capability comparable to that of chatgpt-4.0 in our particular work scenario.

Model	*Compile failed*	*Function failure*	*Good results*
chatgpt-4	8%	24%	68%
chatgpt-3.5	15%	40%	35%
Davinci	26%	56%	18%
fine-tuned Davinci	12%	26%	62%

CONCLUSIONS

Overall, in this work, we attempt to explore the possibility of AI-accelerated verification by automating the construction of property assertions utilizing LLMs, thus freeing verification engineers from the heavy work of assertion writing, accelerating automated assertion generation, and speeding up the FPV process. By designing specific workflows and using asynchronous fifo as the DUT, we provide a preliminary demonstration of the potential of LLMs in automation of assertion generation. Despite the results we have obtained so far, the current big model may not be able to fully realize the good intentions of freeing verification engineers from the tedious task of assertion writing. However, with the continuous development of big model algorithms and more publicly available training data, we believe that big models have great potential to help us achieve this goal.

REFERENCES

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