2021 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA
SHANGHAI | MAY 26, 2021

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Acceleration Startup Design & Verification

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Agenda

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- Enable SW-Driven Verification
- Accelerate Signoff with JasperGold RTL Designer Apps
- Speed Up Verification with Common Methodology For Emulation And Prototyping
- Accelerate SoC Performance Testing with System VIP

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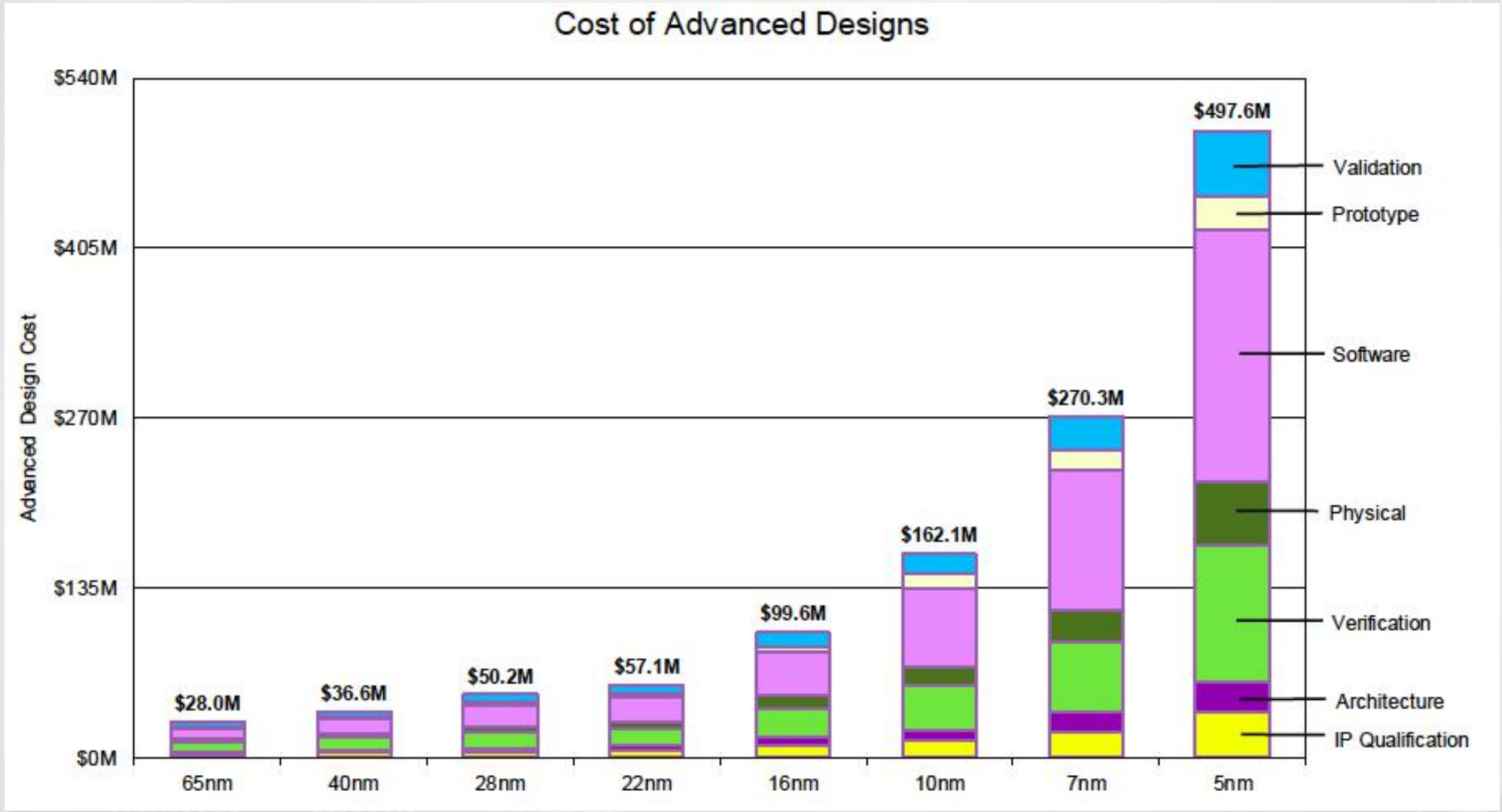
Enable SW-Driven Verification

Software cost is key challenge!

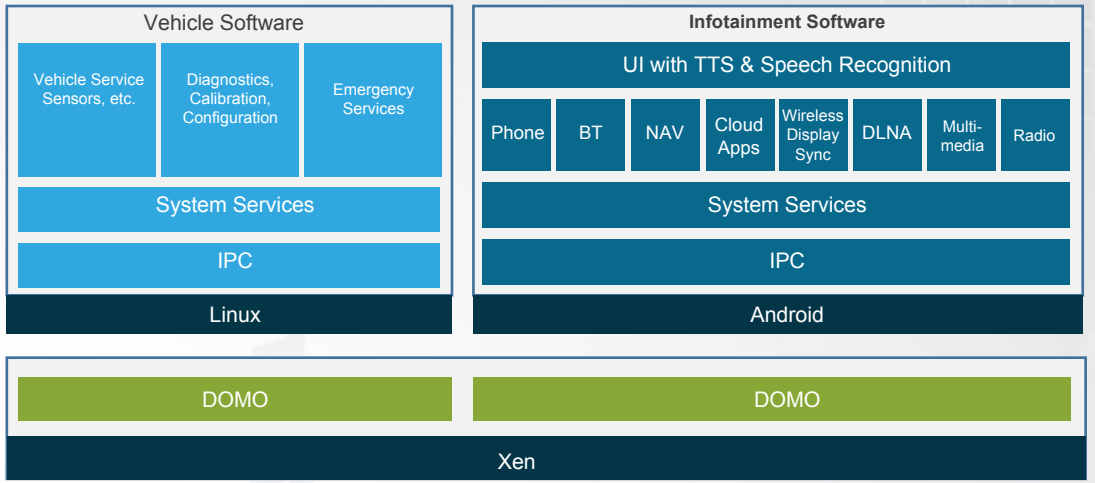


Source: IBS, July 2019

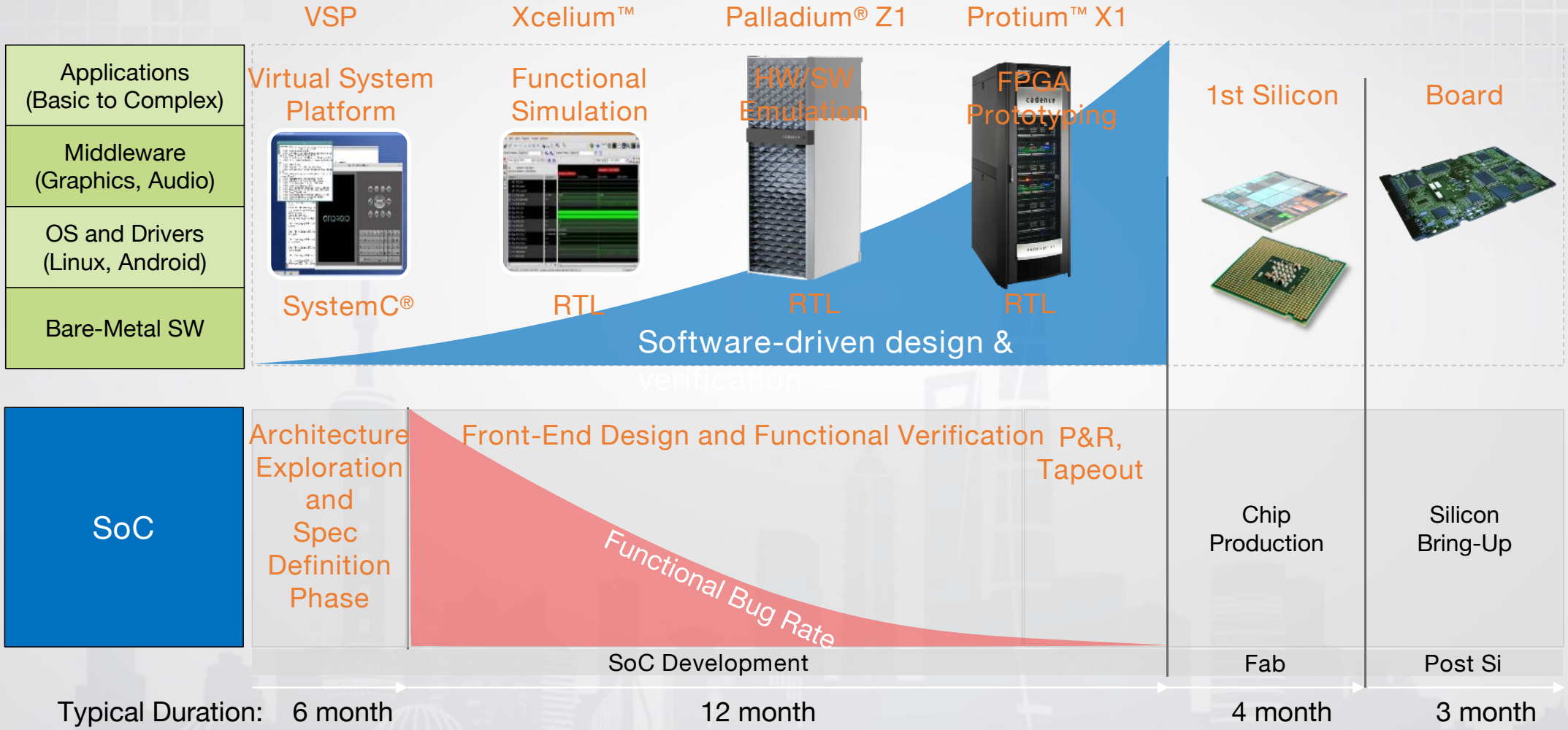
A Lot of Design Details Must Converge Successfully

Software

Hardware



Hardware/Software Co-Verification During SoC Design



Virtual and Hybrid Platform Crucial for Software Speed

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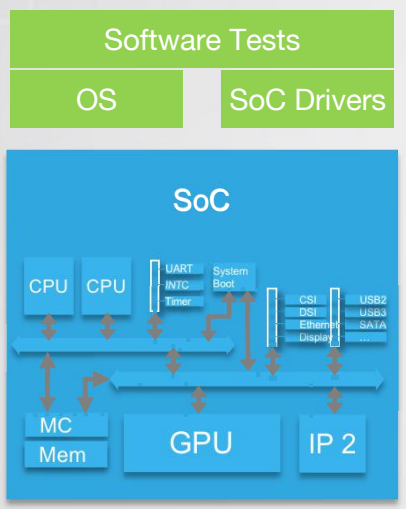
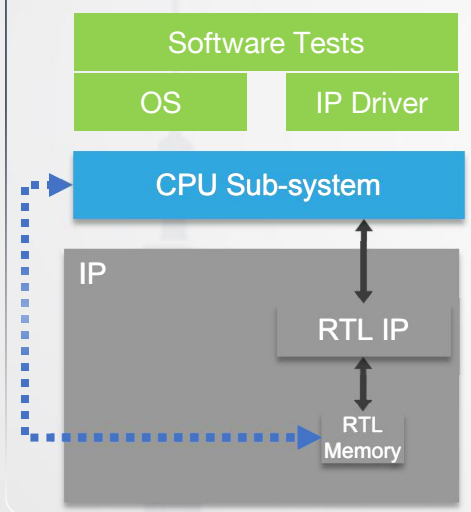
All Virtual

- Pre-RTL SW Development



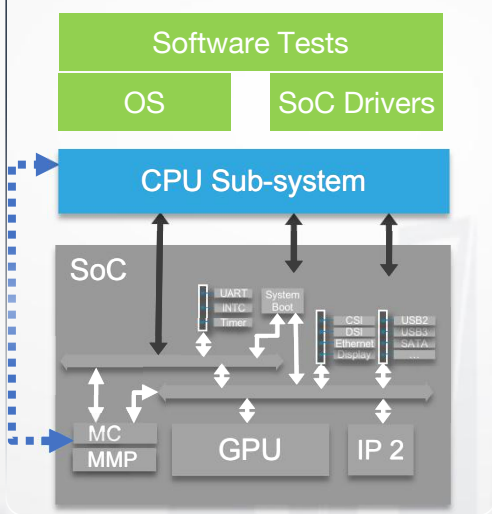
IP Hybrid

- Pre-SoC IP / Driver Validation & Optimization
- RTL – Palladium or Protium



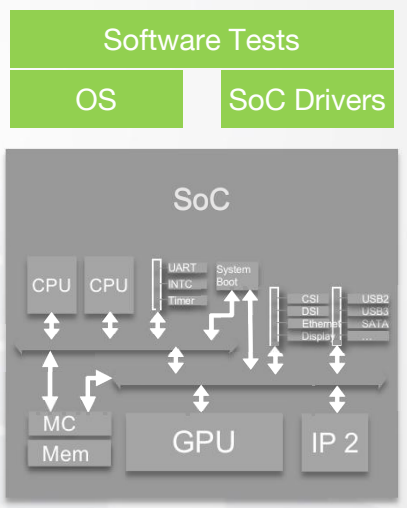
SOC Hybrid

- Pre-Tapeout Hardware/Software Validation



Emulation, FPGA Proto

- Pre-Tapeout Fully Accurate Hardware/Software Validation



All RTL, Silicon

- Final Hardware/Software validation

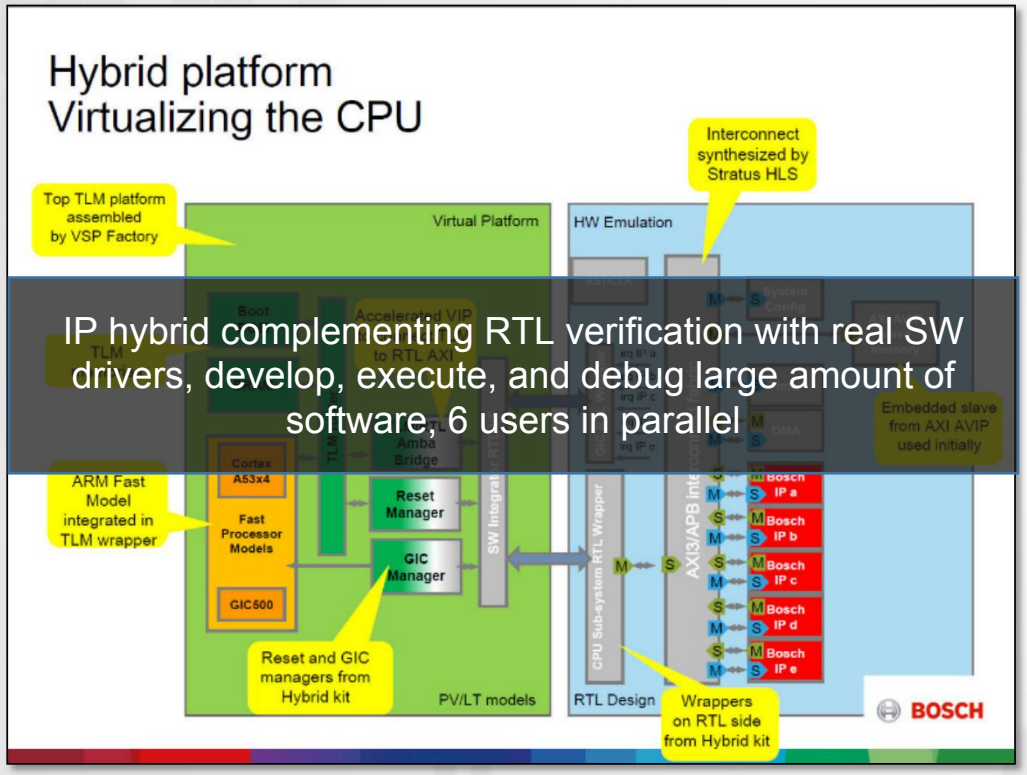
Shift Left

Design

Index

- SW stack
- Virtual Models
- RTL Models

IP and SoC Hybrid Examples



IP hybrid complementing RTL verification with real SW drivers, develop, execute, and debug large amount of software, 6 users in parallel

Source: Emulation Enabling Automotive Designs, http://bit.ly/2yR12r8

SoC hybrid with faster OS boots, smoother SoC bring-up once silicon is back, SW ready to demo product earlier, OpenGL test suites pre-silicon

Source: DAC

Linux >1B instructions
- 2 min with virtualization
- 45 min in RTL

Android >20B instructions
- ~45 min with virtualization
- Hours in RTL

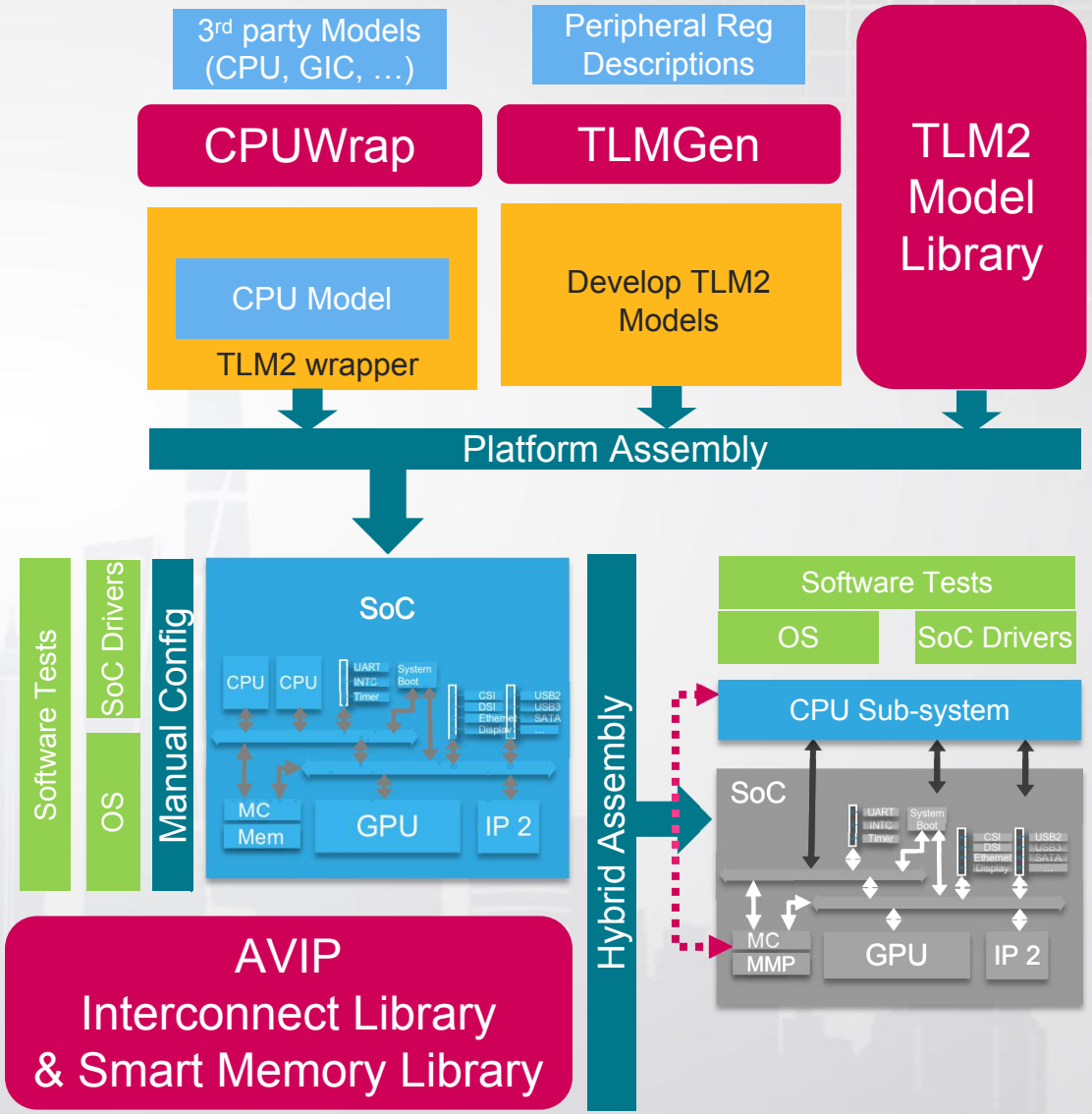
Windows > 50B instructions
- ~80 min with virtualization
- Days in RTL

PreSilicon Software Validation Focus

- Fastest software execution across engines
  - Leveraging abstraction and connecting fastest engines
- Native software debug and configuration across engines and abstractions
  - Assembly and configuration for virtual and hybrid
  - Native SW debug across abstractions and run time engines
- Open platforms and models
  - Virtual Models based on standard SystemC TLM2
  - Run time / control framework natively integrated with a heterogenous model ecosystem
  - Tightly integrated with Cadence platforms – Palladium, Protium and Xcelium.

Leveraging Abstraction for Performance

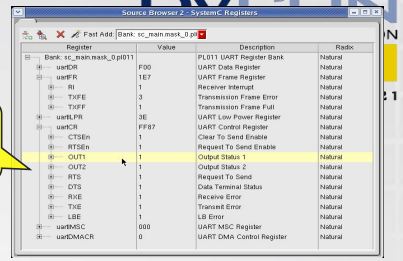
- Virtualization (Models)
  - CPU and Interrupt Controller selection is key
  - Leverages TLM2 Direct Memory Interface (DMI)
  - Virtualize High Activity Peripherals
    - Timers, UARTs, Interrupt Controllers, …
- Virtual Reference Platform
  - Reference Platform running required software
    - Platform completeness depends on requirements
  - Start from required software and work back
    - Android -> which cpu -> which interrupt controller
  - Existing reference platforms
    - Android 9 and 10, Linux Multi-core, …
- Hybrid
  - Connecting Virtual Platform to RTL (Palladium/Protium)
  - Which interconnect, smart memory, …



Virtual Prototype Model Generation

Modeling Time Spent on Functionality

Register Window GUI



IP-XACT or RDF

TLM Interface Generator

Register Descriptions & Configuration Options

- Cadence RDF
- IP-XACT

IP-reg.h — C-API for firmware register access

IP-test.c — Pin change & IP register read/write test software

Reg.txt — Register and IP function documentation

IP.CC — TLM 2.0 I/O, register definitions, and read/write functions

IP.CC

* Register read/write functions { Functionality (…); }
* Pin change functions
* Reset functions

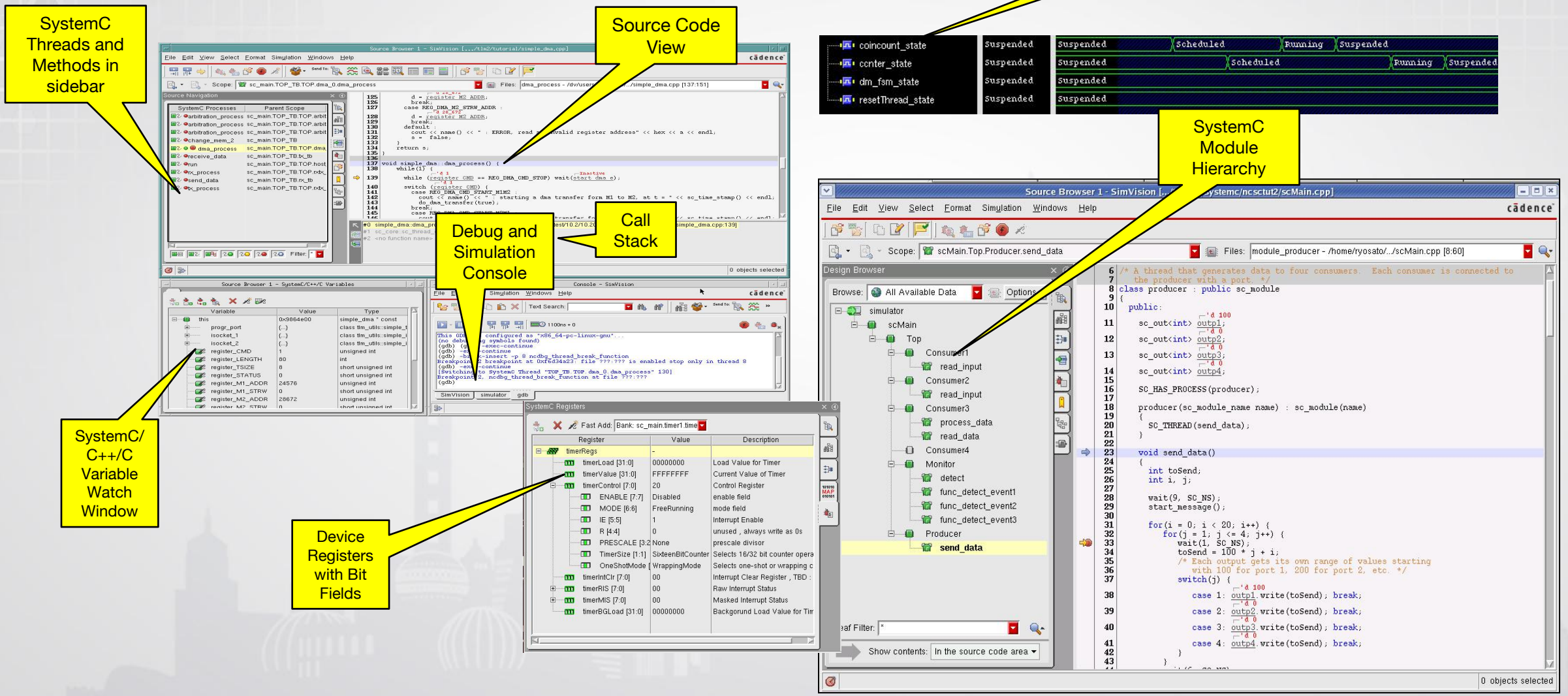
Generated TLM 2.0 software

OR

Func.CC — Source functionality

*.o — Binary models

Virtual Platform Debug
SystemC/TLM Aware Debug



Unified Hardware / Embedded Software Debugging

Fully Transparent and Integrated Across Both Domains

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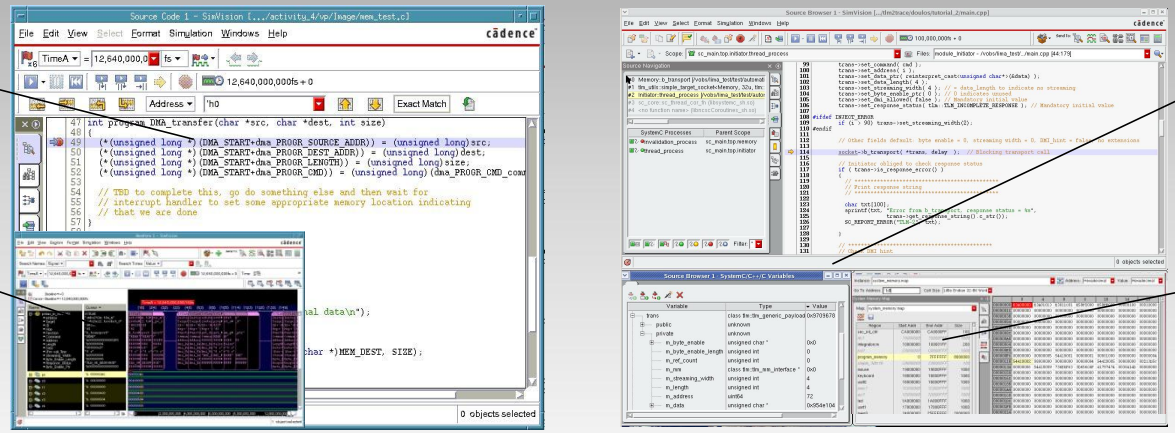
Combined Software / Hardware Debug View

Software Debug View

Hardware Debug View

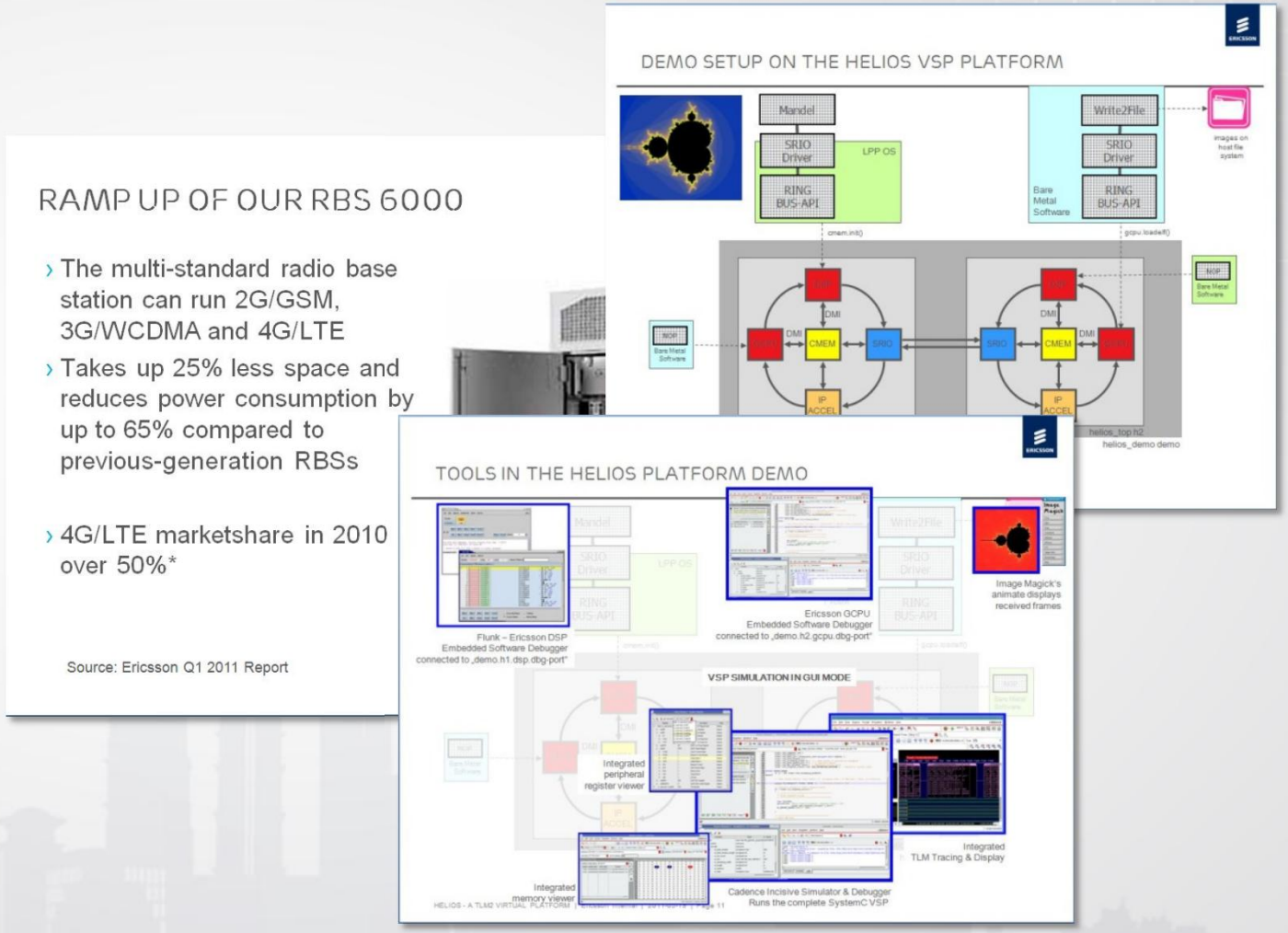


- Set break points in either hardware or software
- Single step in hardware or software
- Debug individual cores in multi-core system
- View register and memory views for each core

Ericsson use of Cadence Virtual System Platform

CadenceLIVE & DVCon

- Ericsson RBS 6000 Basestation
- Ericsson Helios Virtual Platform
  - Enables software developers to immediately begin SW development
  - High performance abstract TLM models available months before RTL



Intel Mobileye – Early SW development

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Challenges in Pre-Silicon SW validation

- Software validation has a big impact on "time to market" of automotive products
- Pre-Si SW validation in HW/SW co-sim ensures a high SW quality on silicon arrival
- Requirements to shorten the SW turnaround time on Si:
  - Fast bring-up / High execution frequency / Quick turnaround time / Accuracy / Debug
- What is the best Pre-Si platform for fast SW convergence?
- What is the right methodology for the job?

Platform	Benefit	Limitation
Virtual Simulator	Early, fast, high debug	Timing accuracy, not all IP available/effort porting IP to TLM models no co-verification of SOC – RTL/SI
RTL Simulator	Accurate, high debug	Extremely slow, impossible for complex software runs
RTL Emulator	Accurate, high debug	x1000 faster than RTL but still not enough for SW convergence

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Hybrid advantages from the SW programmer's point of view

- vs. Pure Emulation
  - Dramatically reduced boot time
  - Interactive mode of operation, control OS (Linux) via console
- vs. Pure Simulator
  - Much more precise model
  - No need to develop any model for peripherals
- vs. Silicon
  - Schedule "Shift-Left": SW enablement before Silicon arrival
  - Enable error injection to test software bad path scenarios
  - Convenient waveform debug of HW signals/register values (key to debug HW/SW issues)

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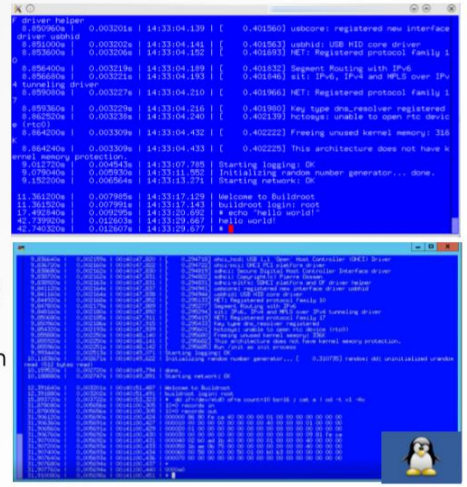
Results

- Full Linux OS boot in 32 seconds instead of 2-3 hours on non-hybrid emulation
- High level of software validation and readiness even before Si arrival
- Validate complex software and complex scenarios
- Validate SW drivers for peripherals in OS context: OSPI, eMMC and PCIe on RTL
- Shorten SW bring up time for Si
- User friendly environment for both HW and SW debug
- Same SW image used as for pure emulation
- Quick retest of new SW image
- Gate count of hybrid design is 37% lower



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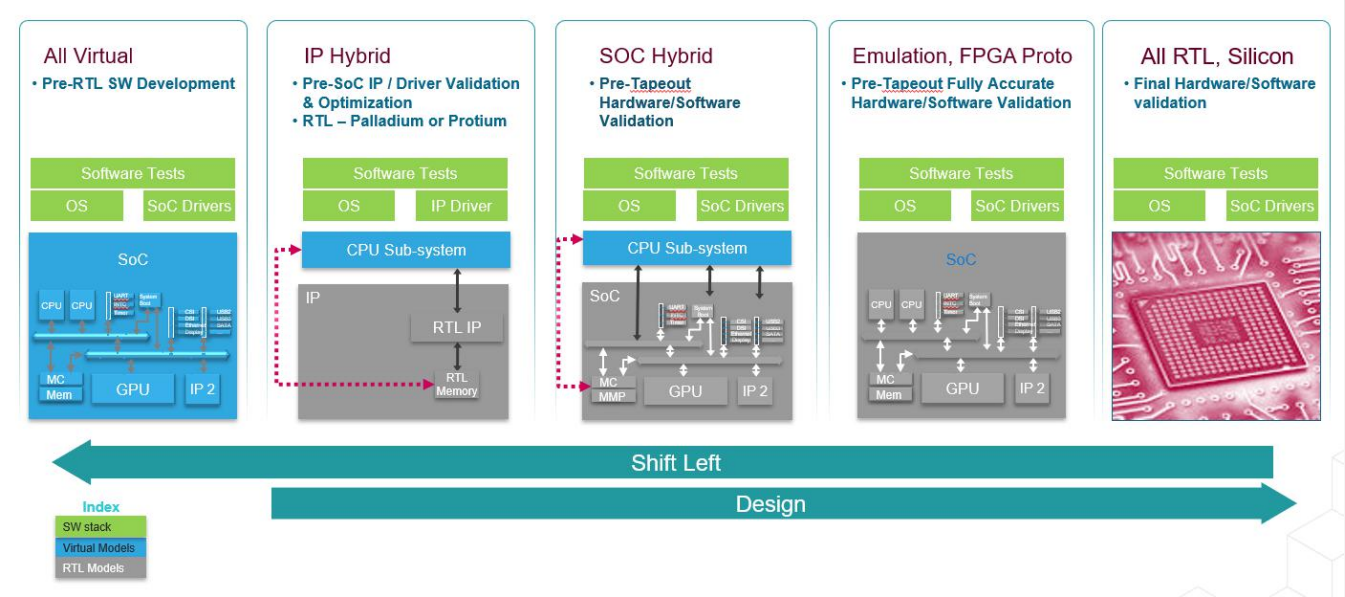
Commitment to Software-Driven Verification



- Enable early SW development and validation
  - Based on SystemC models or CPU fast models
  - When only some key IP(s) ready
- Native software debug and configuration across engines and abstractions
  - Assembly and configuration for virtual and hybrid
  - Native SW debug across abstractions and run time engines
- Open platforms and models
  - Virtual Models based on standard SystemC TLM2
  - Run time / control framework natively integrated with a heterogenous model ecosystem
- Tightly integrated with Cadence platforms – Palladium, Protium and Xcelium.
- Fastest software execution across engines

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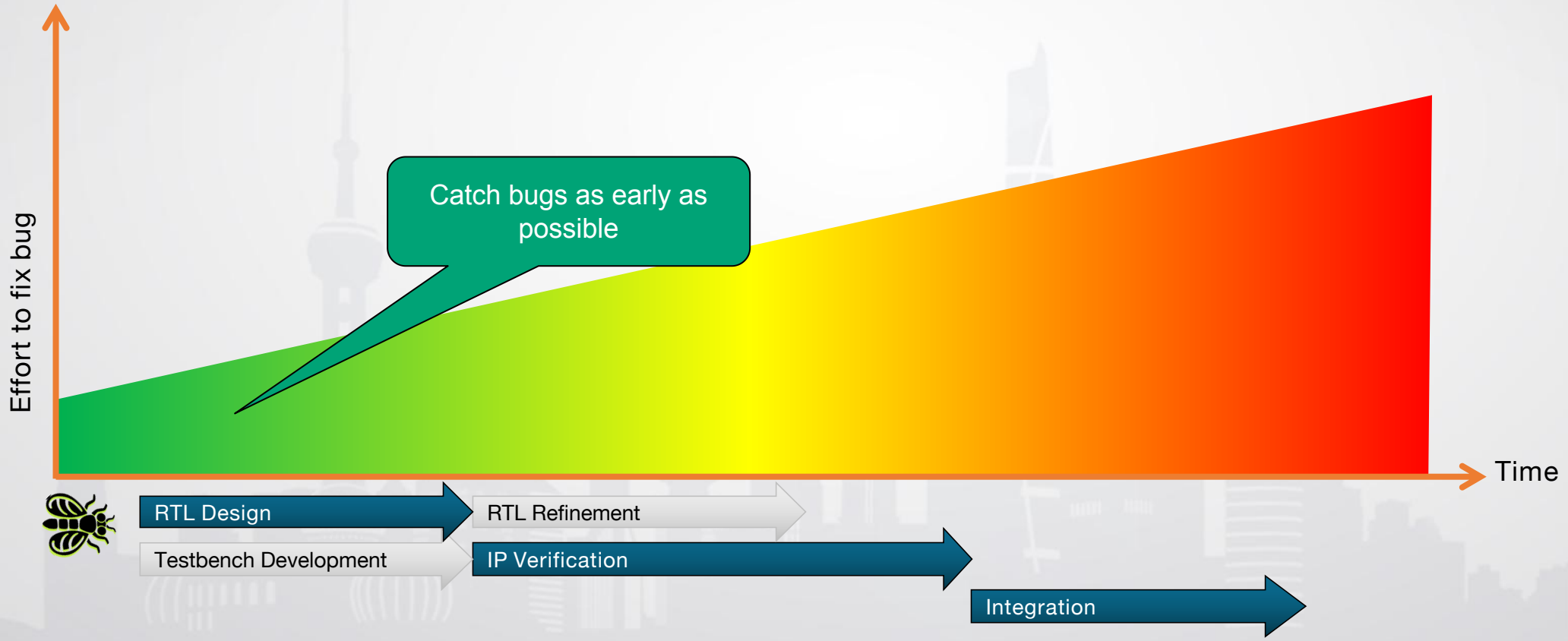
Accelerate Signoff with JasperGold RTL Designer Apps

Need for Early Design Checking

- Effort and cost to fix a bug increases significantly further into the development cycle



RTL Signoff by Designers: Big Picture

- Typical RTL signoff includes
  - Signoff the RTL against a comprehensive set of structural lint/DFT/CDC/RDC checks
  - All checks are 'automatic' and user provides RTL + constraints (for DFT and CDC/RDC)

AUTOMATIC STRUCTURAL CHECKS

- For comprehensive signoff, augment with automatic functional checks
  - High-value code reachability and functic
  - Functional CDC/RDC checks

AUTOMATIC FUNCTIONAL CHECKS

- JasperGold® platform uniquely positioned t solution for

AUTOMATIC STRUCTURAL CHECKS

+

AUTOMATIC FUNCTIONAL CHECKS

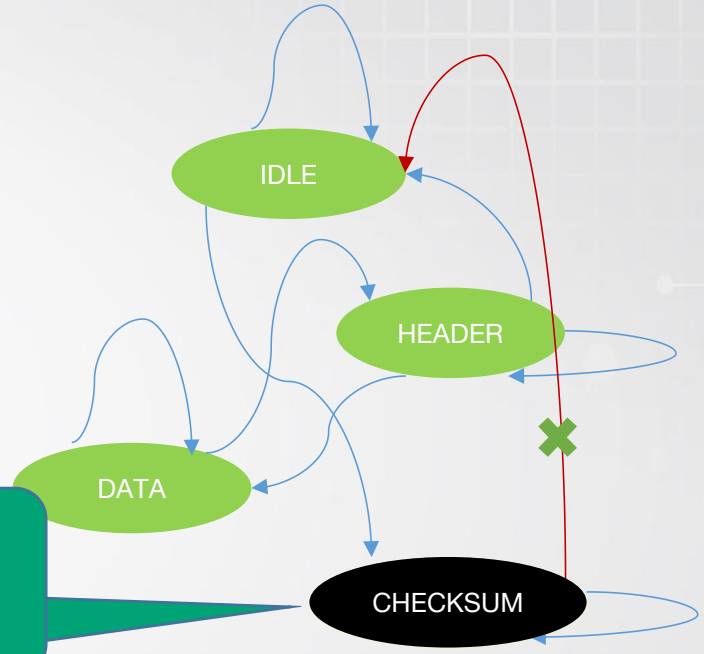
Auto-Formal Checks: FSM Reachability/Deadlock Example

- Structural LINT cannot catch such issues
- These issues are high value to caught at RTL stage and can be automatically checked using auto-formal checks

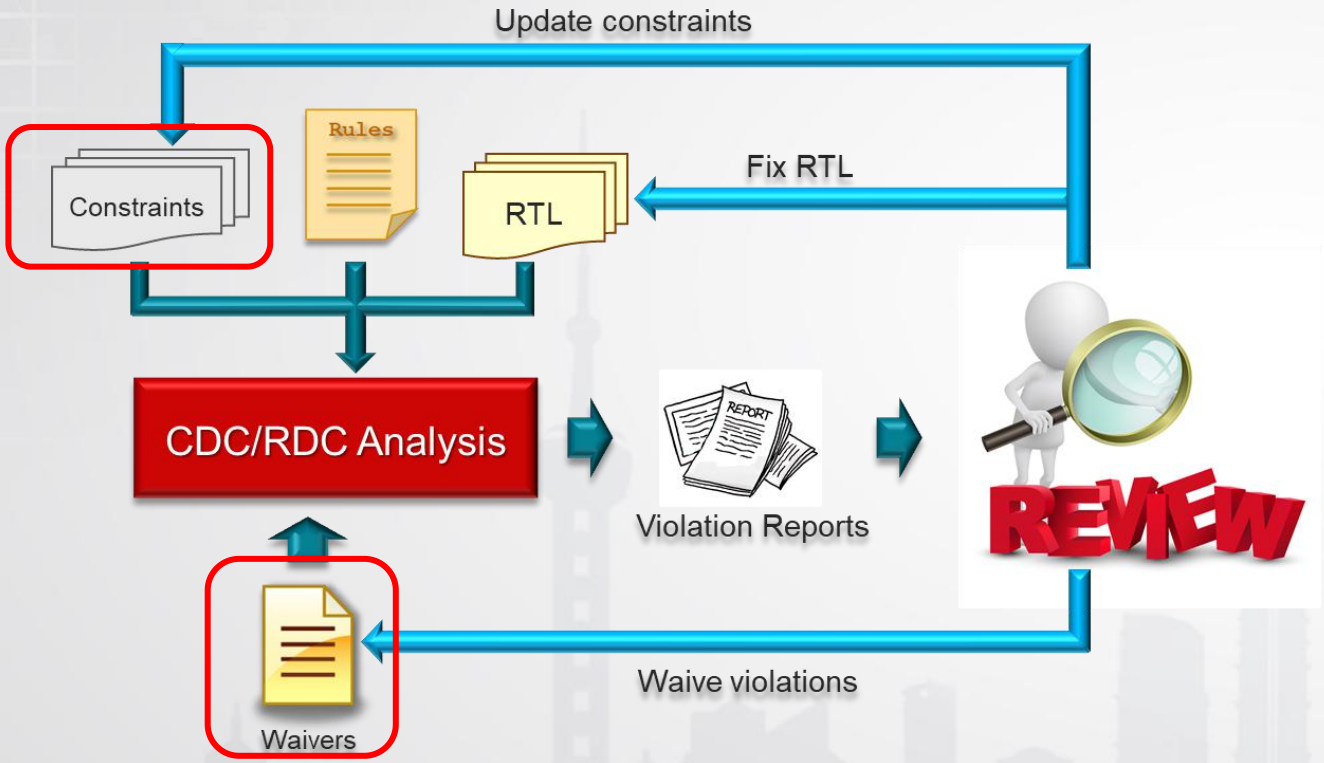
```
always_comb begin
    parse_st_nx = parse_st;
    if (enq_valid) begin
      case (parse_st_nx)
        IDLE: begin
          if (enq_sop) parse_st_nx = CHECKSUM;
        end
        HEADER: begin
          if (word_cnt == cfg_header_length) parse_st_nx = D
          else parse_st_nx = HEADER;
        end
        DATA: begin
          if (enq_sop) parse_st_nx = HEADER;
        end
        CHECKSUM: begin
          if (enq_sop_id) parse_st_nx = IDLE;
          else parse_st_nx = CHECKSUM
        end
      endcase
    end else begin
      parse_st_nx = IDLE;
    end
end

always @(posedge clk_header or negedge rstn) begin
  if (!rstn) begin
    header_valid <= 1'b0;
  end else begin
    header_valid <= enq_valid && (parse_st_nx == HEADER);
    header_data <= enq_data;
  end
end

always @(posedge clk_payload or negedge rstn) begin
  if (!rstn) begin
    payload_valid <= 1'b0;
  end else begin
```



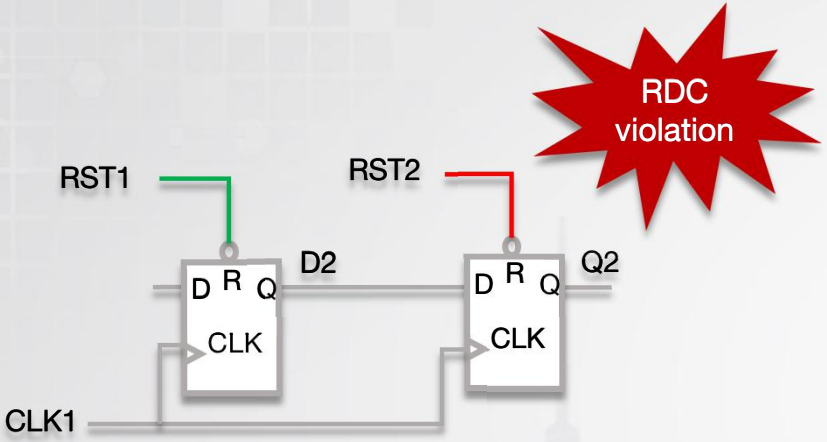
Domain-Crossing Verification – Gaps in Conventional Flow



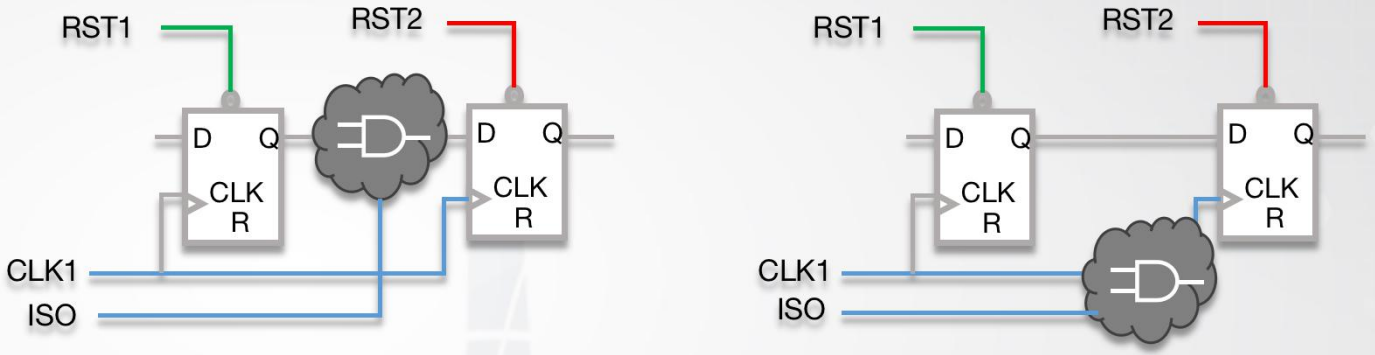
1. Correctness of analysis constraints
   - User-specified constraints are considered golden
   - Reuse of constraints – a big source of bugs
   - Are my constraints correct?
2. Validity of waivers
   - Assumptions made about design functionality
   - Reviewed based on waiver comments
   - Are the underlying assumptions for my waivers valid?
3. Metastability-aware verification
   - How do I guarantee that my design is immune to metastability effects?
   - Is my functional verification environment metastability aware?
   - Generally modeled with randomized synchronizer delay in simulation – Pessimistic and incomplete

Linking CDC/RDC analysis with functional verification is the key

Validity of Waivers



Reset Domain Crossing



Reset Isolation Strategies

- RDC violation: Destination flop (`Q2`) may go metastable if source reset (`RST1`) is asserted while destination reset (`RST2`) is de-asserted
- Considered safe if reset isolation logic is present
- Assumption: The RDC path (`D2`→`Q2`) cannot be sensitized when reset isolation is active
- Is this assumption valid?

Missing verification linkage to validate waiver related assumptions

JasperGold Superlint App

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Structural Lint and DFT Checks

+

Automatic Formal Checks

DFT controllability

Sim-synth mismatch

Naming

Coding style

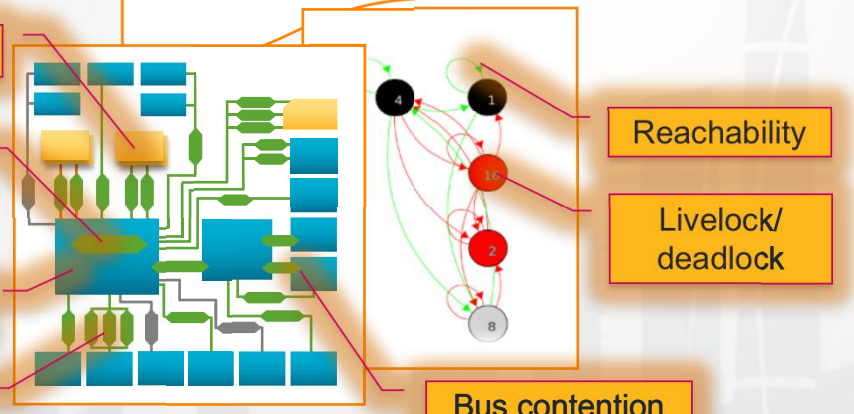
DFT observability

X assignment

Arithmetic overflow

Range overflow

Combo loop analysis



Reachability

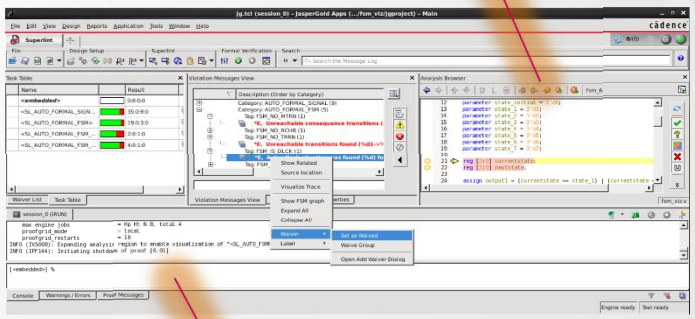
Livelock/ deadlock

Bus contention

Enabled by true formal technology

Best-in-class debug

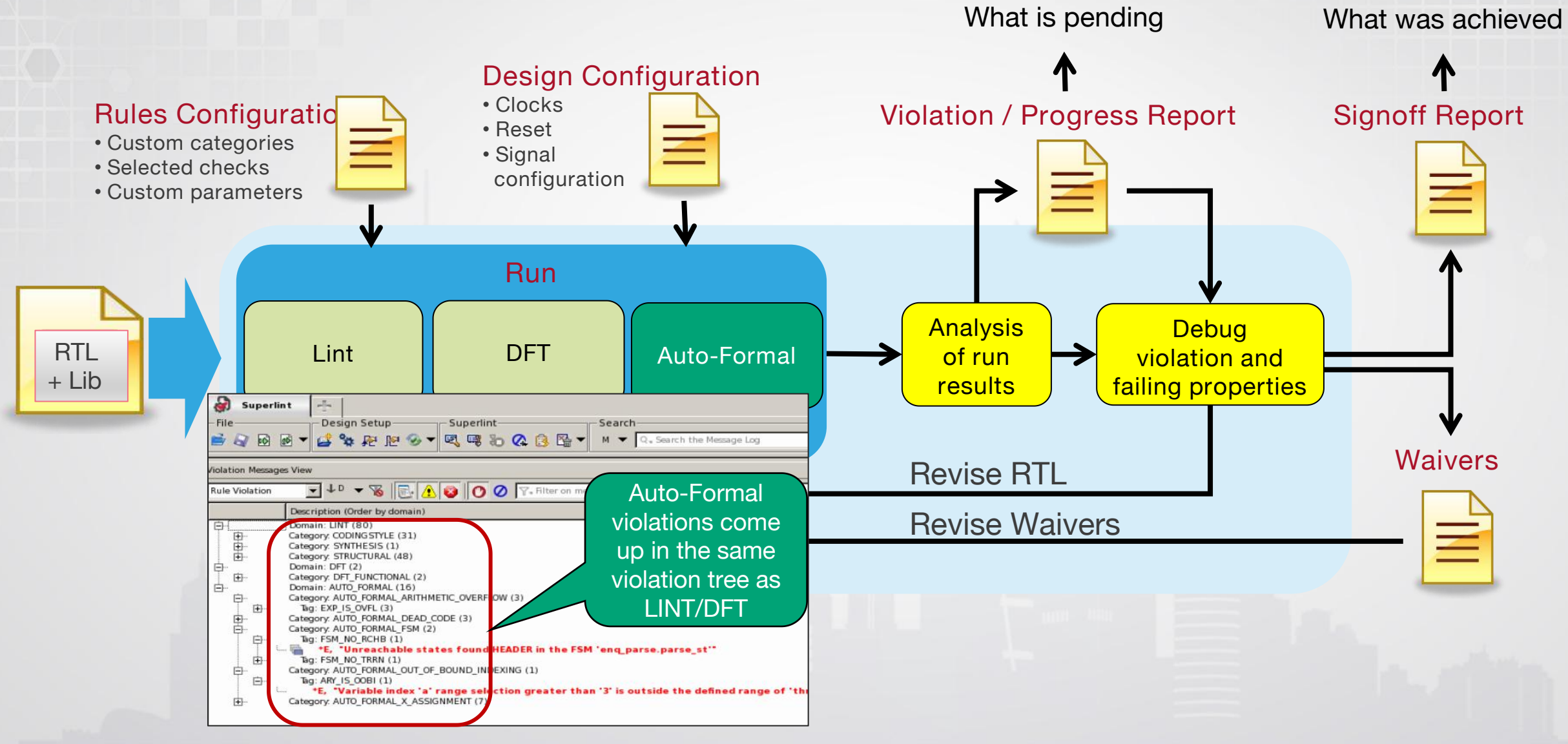
JasperGold® Visualize™ Environment



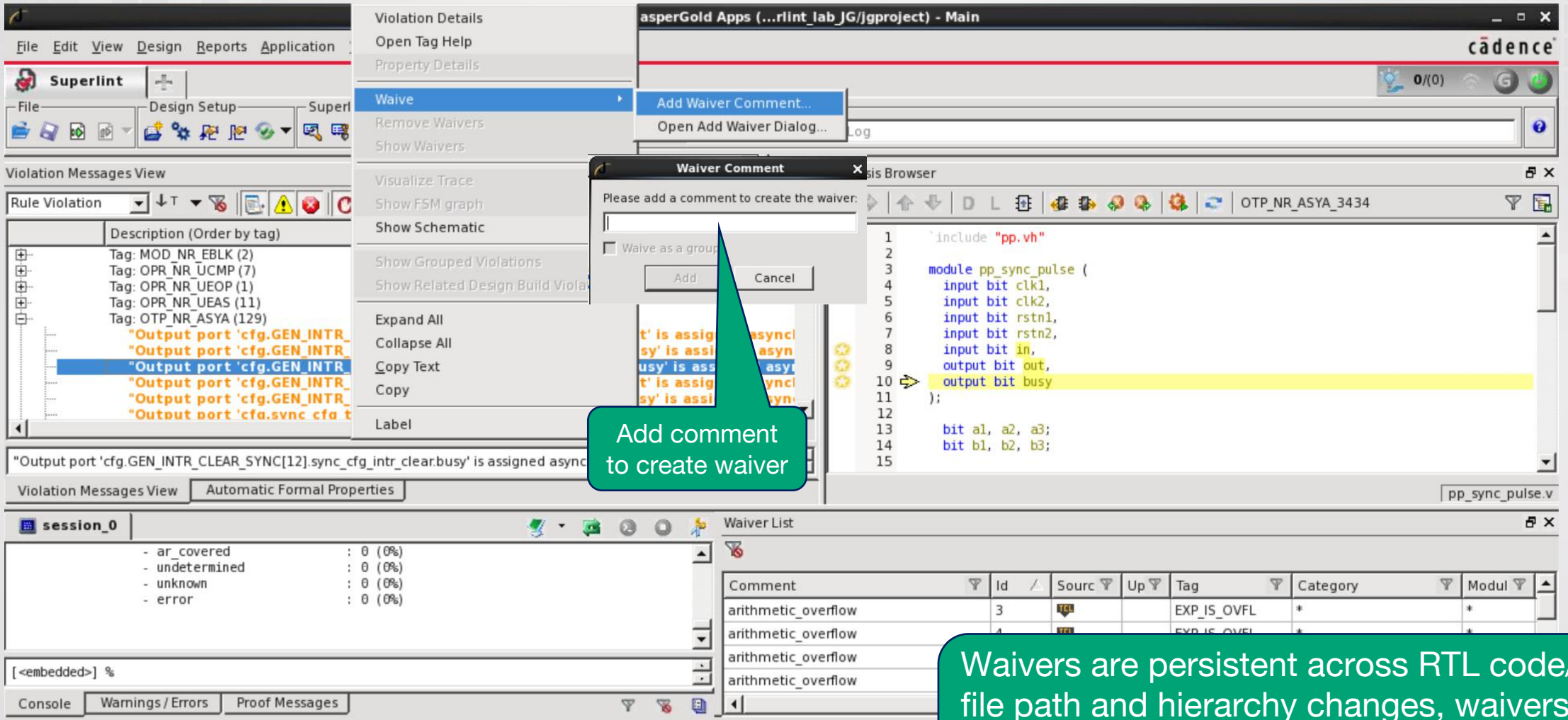
Low-noise violation and waiver handling

Comprehensive functional checks, violation debug, and waiver handling based on best-in-class formal analysis

Superlint Flow

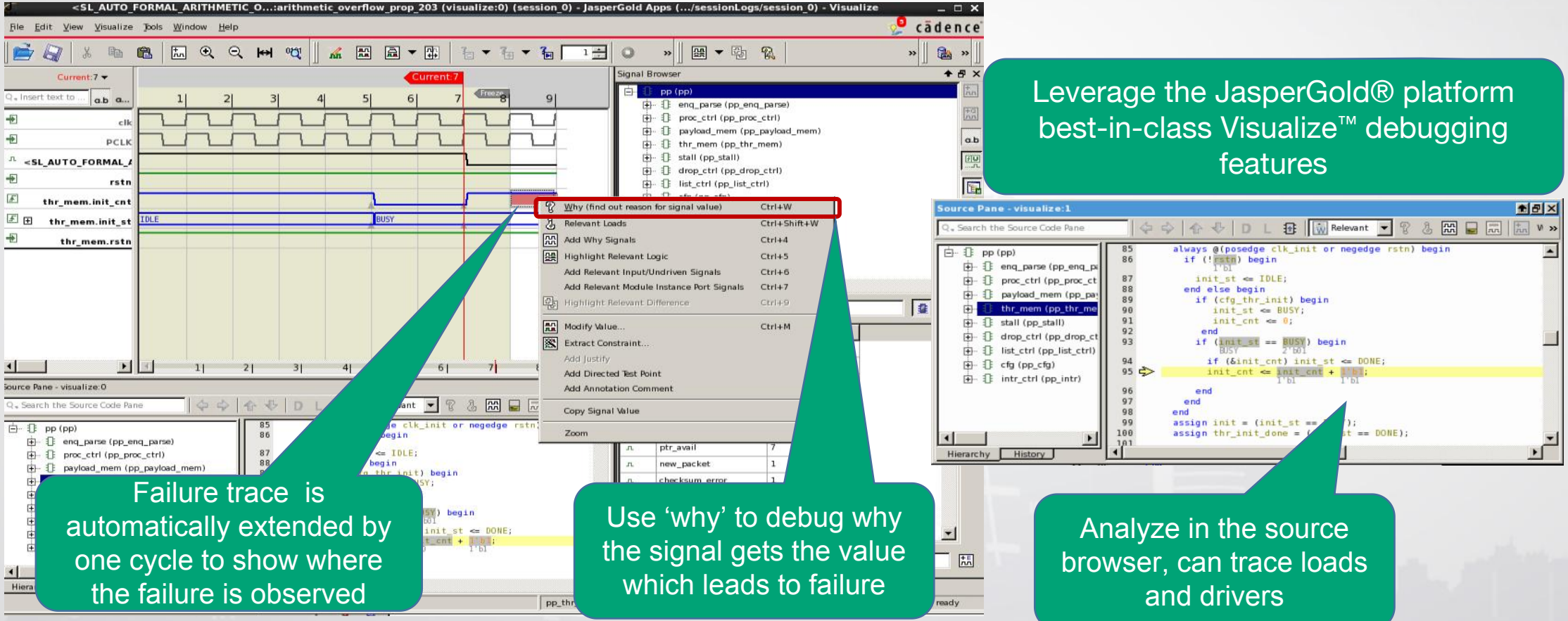


Persistent Waivers



Observability-Enabled Debug

- Debugging auto-formal violations show where the violation propagates
  - Boundary signals are added to the debug window
  - The propagation cycle is highlighted – hints the user to perform “why”



JasperGold CDC App - The Complete Picture

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Enabled by true formal technology

Comprehensive Checks

Wide range of synchronizers (NDFF, Mux, FIFO, Handshake, User-defined…)

Automatic structural checks

Functional checks (Gray, FIFO…)

Clock/Reset Tree

Convergence/ Glitch

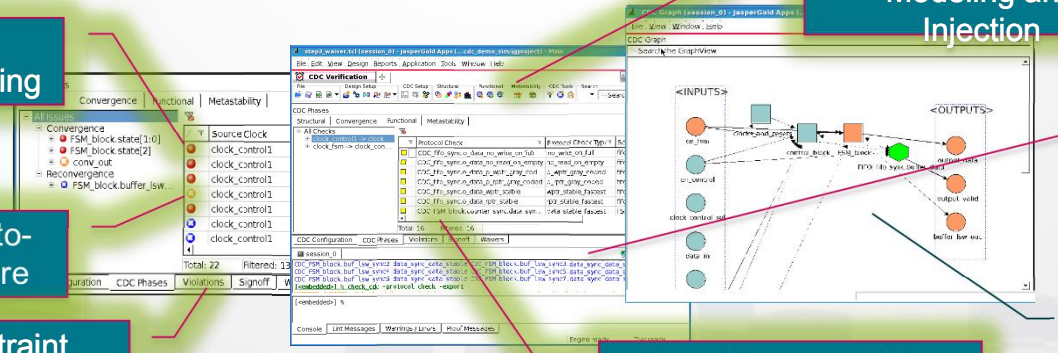
+

Metastability-Aware Verification, Innovative Debug, and Waiver Handling

Low-noise violation handling

Powerful auto-waiver feature

Constraint Validation



Metastability Modeling and Injection

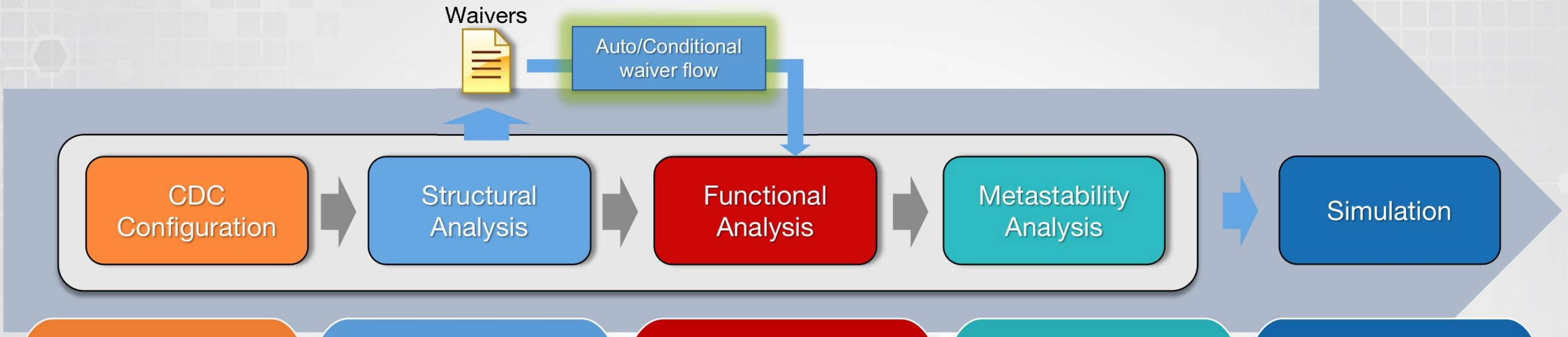
Metastability Injection in Simulation

Assertion generation and export to simulation

Innovative debug with Visualize™ and Graph views

The only CDC solution with industry-leading formal technology for functional checks, asynchronous verification, and waiver handling

True CDC/RDC Signoff Flow with JasperGold CDC App



- Clock specifications
- Reset specifications
- Signal configurations

- Clock/reset tree checks
- CDC synchronization checks
- Convergence/glitch checks
- Reset synchronization checks
- Reset domain crossing checks

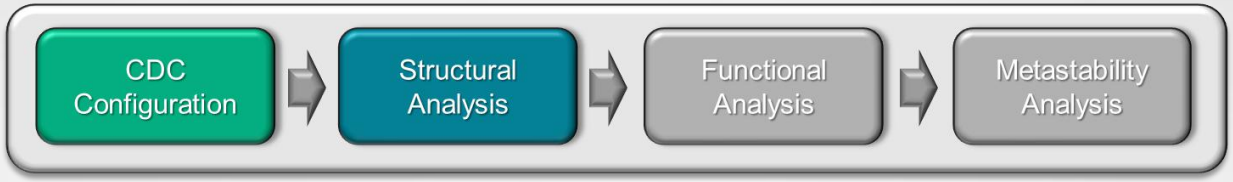
- Signal configuration validation
- Clock relationship checks
- Reset order/priority checks
- CDC protocol checks
- Waiver condition validation

Metastability-aware proof of:

- User-written assertions
- CDC protocol checks
- Waiver conditions

- Metastability-aware simulation
- CDC protocol checks
- Signal config checks
- Waiver conditions

CDC Configuration and Structural Analysis



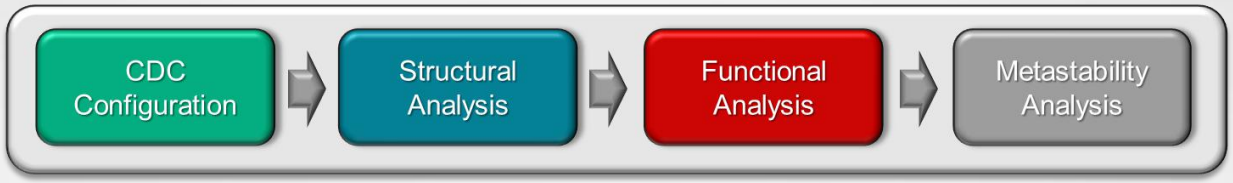
- CDC configuration
  - Specify clock properties and relationships (using SDC or native commands)
  - Specify correct reset types (async/synchronized/synchronous) and reset priority
  - Declare signal configurations (constant/static/mutex/gray-code) with conditions
- Comprehensive structural analysis
  - Clock and reset tree checks
  - CDC synchronization checks
  - Convergence/glitch checks
  - Reset, RDC checks
  - Waivers added while dispositioning structural violations

Garbage In = Garbage Out

Wrong Waivers = Masking Is

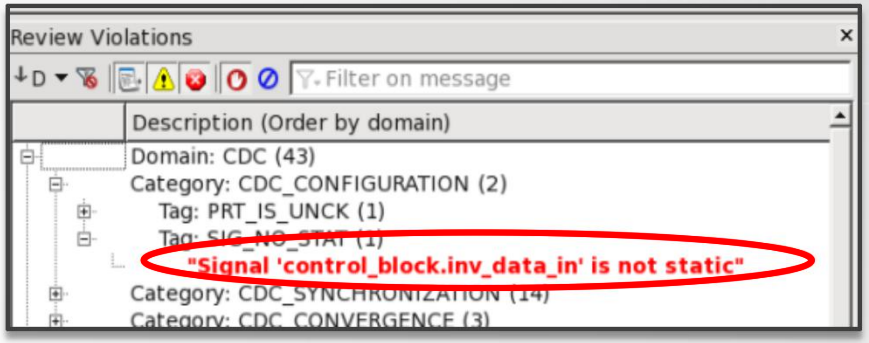
Signal configuration correctness and waiver-related functional assumptions should be verified

Functional CDC Analysis



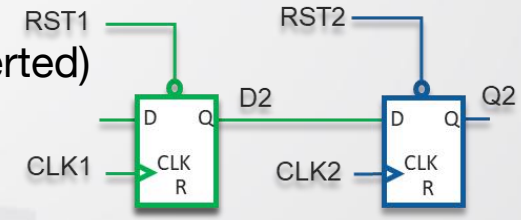
Signal configuration validation

- Auto-generated assertions for verification
- Proven in formal verification environment



Verify ***pseudo*** nature of constraints

- Specify triggering event for signal to be constant/static
- Example:
  - Data on CLK1 domain can change only when destination is in reset (RST2 is asserted)
  - `check_cdc -signal_config -add_static D2 -condition RST2`
- Additional verification to ensure pseudo-static property



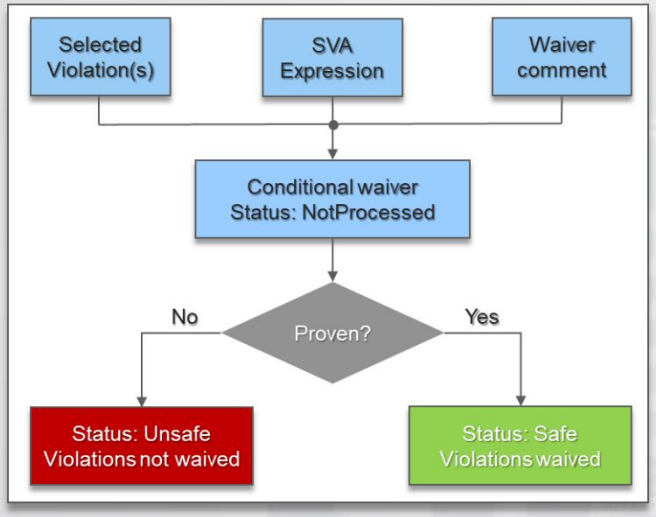
Export and run signal configuration checks in simulation

Verification of analysis constraint correctness leads to greater confidence!

Functional CDC Analysis (cont)

Functional Analysis

- Waiver condition validation
  - Validation of functional assumptions used in dispositioning structural violations
  - Auto-waiver flow
    - Tool automatically detect conditions for dispositioning structural violations
    - Violations are waived if the condition is proven
    - Example: Gray encoded buses, unsynchronized paths but are metastability safe
  - Conditional waiver flow
    - User provides SVA expression for waiver condition
    - User-selected violations are waived only if the condition is proven




```
% check_cdc -waiver -add -filter ..............
          -comment "stable Q2 during RST1"
          -expression {##1  $fell(RST1) && $stable(RST2) |-> $stable(Q2)}

% check_cdc -waiver -prove
```

Verification reduces noise and avoids errors in manual dispositioning of violations

Metastability Injection (MSI) Flow in Formal

- Pre-requisite: Formal Property Verification (FPV) environment
  - Passing functional assertions
- Push button flow with customized debug in visualize
  - Inject metastability in user properties
  - Verify user-defined properties in presence of metastability
- Metastability awareness in protocol checks

MSI Flow in Simulation

- Pre-requisite: Simulation environment with passing test cases
- Simple, easy to use, no instantiation flow in simulation
  - Timing violation monitors and injection modules exported from JasperGold® platform
  - Injection models can mimic both setup and hold violations
  - Not dependent on synchronizer types – all CDC crossings covered
  - Configurable setup, hold time windows for individual clocks
- Random/Always/No Injection modes

Conclusion

- JasperGold® Superlint App is industry-leading solution for RTL signoff by designers
  - ✓Comprehensive structural LINT and DFT checks
  - ✓High-value auto-formal checks
  - ✓Easy setup and feature-rich analysis and debug environment
  - ✓Designed to be low-noise, high-productivity application
- JasperGold® CDC App is a holistic CDC/RDC verification solution
  - ✓Comprehensive structural checks
  - ✓Functional CDC/RDC verification
    - Constraint validation
    - Waiver validation
    - CDC protocol verification
  - ✓Metastability-aware verification

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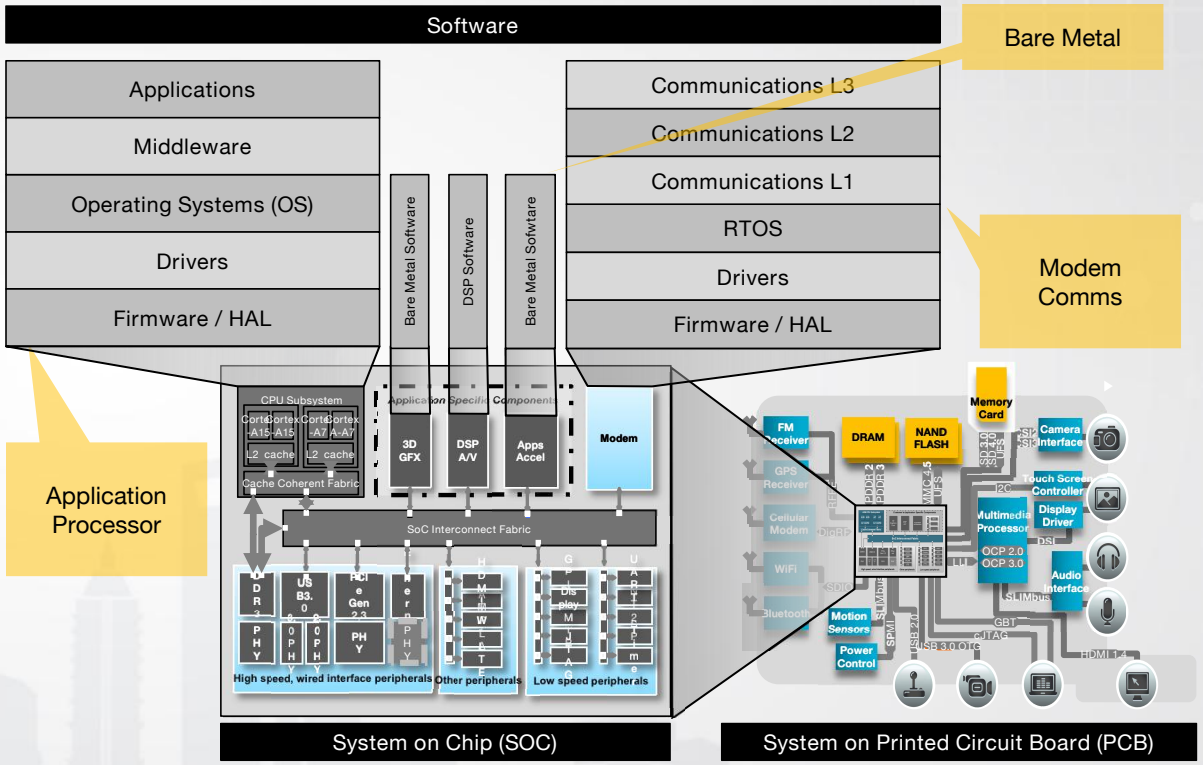
Speed Up Verification with A Common Methodology For Emulation And Prototyping

list the Authors and affiliations here

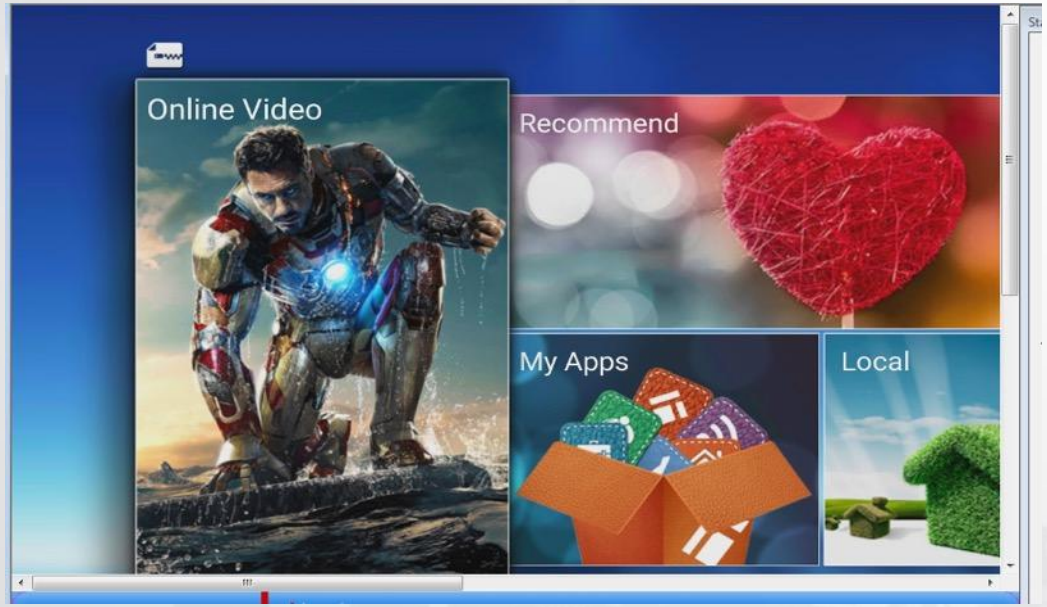
System & Chip design trend 2021 - 2025

- Time-to-market
- Development cost reduction
- Multi-core design and verification complexity
- Integration of new designs and derivatives
- Software stack development
- Hardware-software convergence
- More than 80% re-use
- More than 60% of effort in software

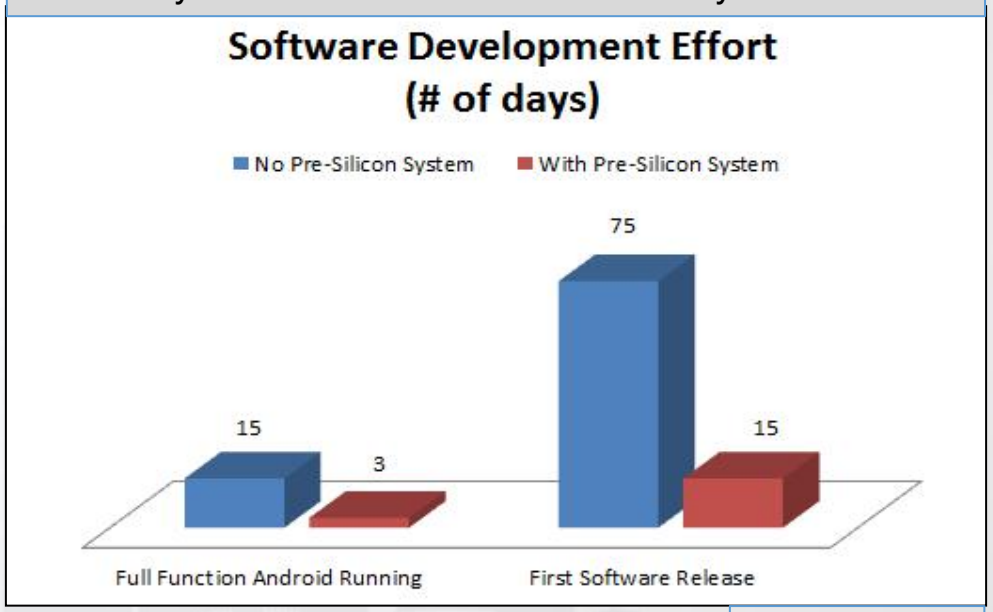


Emulation & prototyping accelerate time to product (revenue)

- Early, embedded software & firmware development
- Initial systems and/or proof of concept
- Pre-silicon chip (ASIC) verification

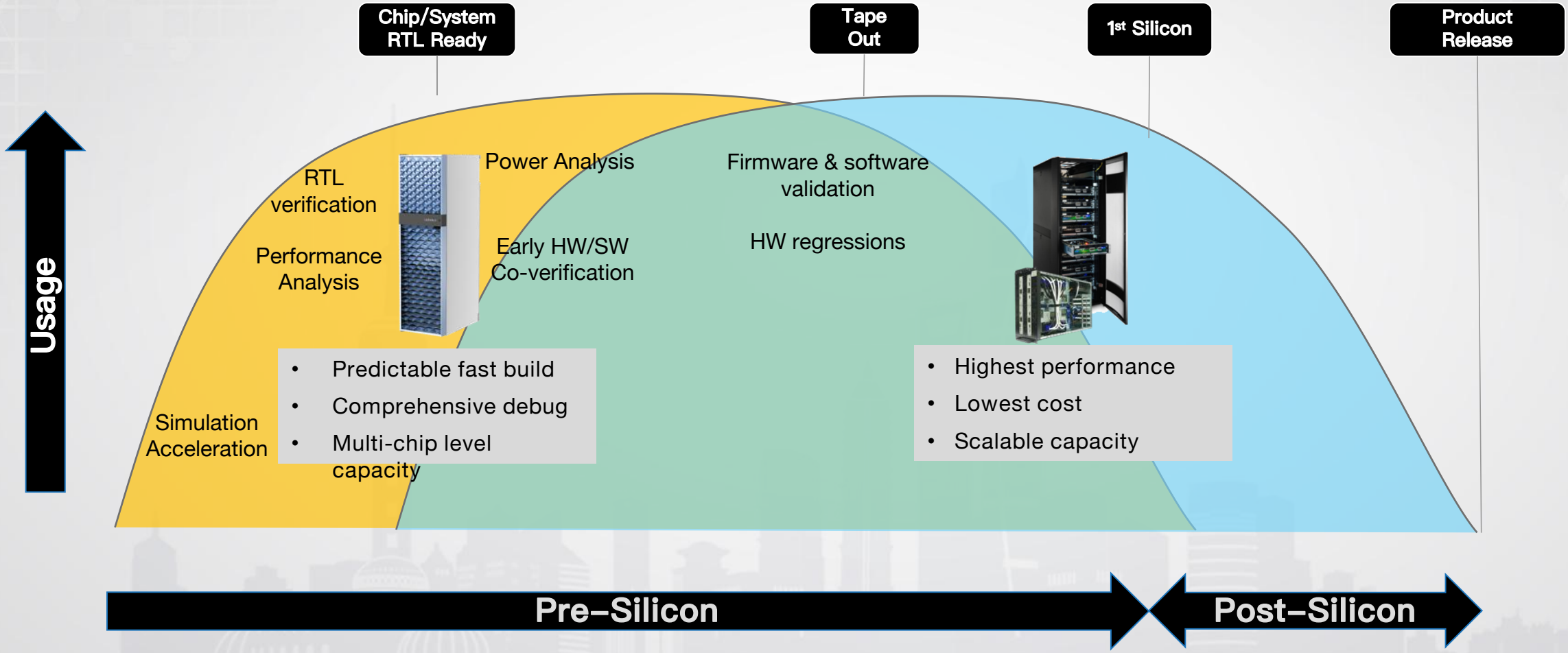


Software is ready when 1st silicon comes in
- Full Android boot 30 min after silicon is back
- Full system demo to customer in 3 days

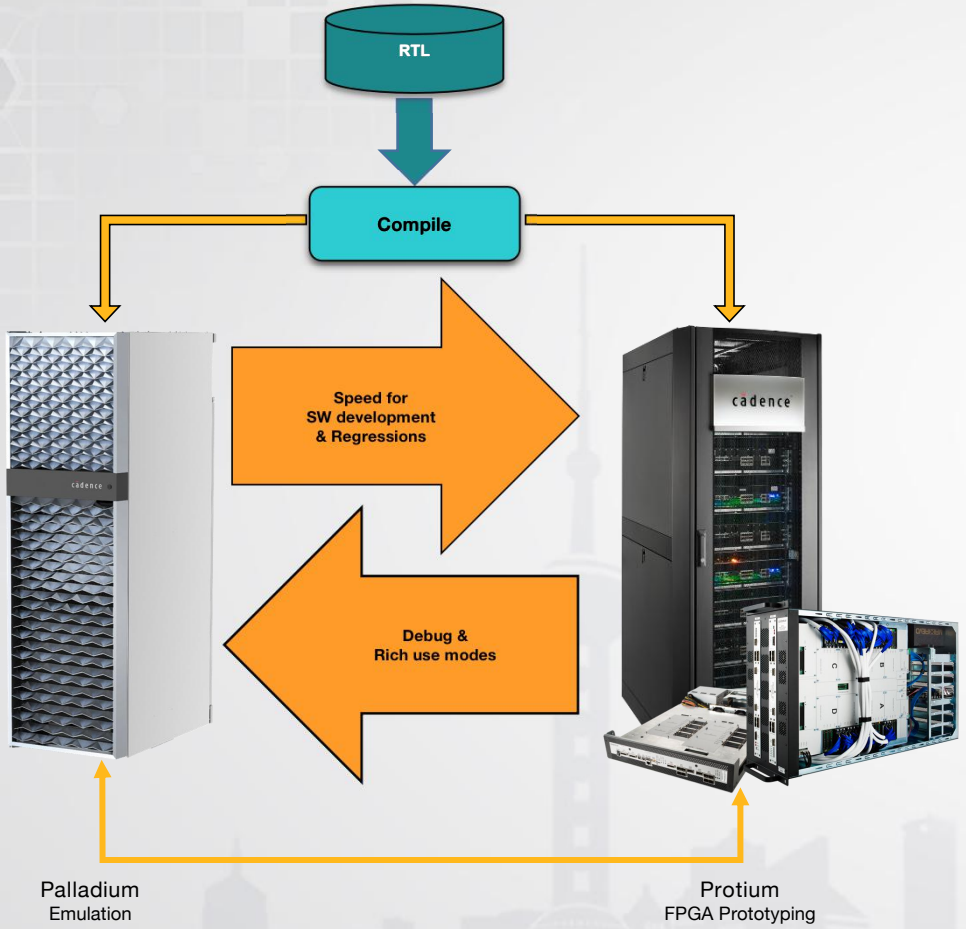


Source: Amlogic

The Right Tool, for the Right Job, at the Right Time!



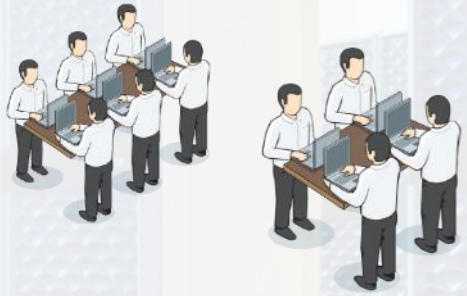
Palladium Z1 to Protium X1 benefits



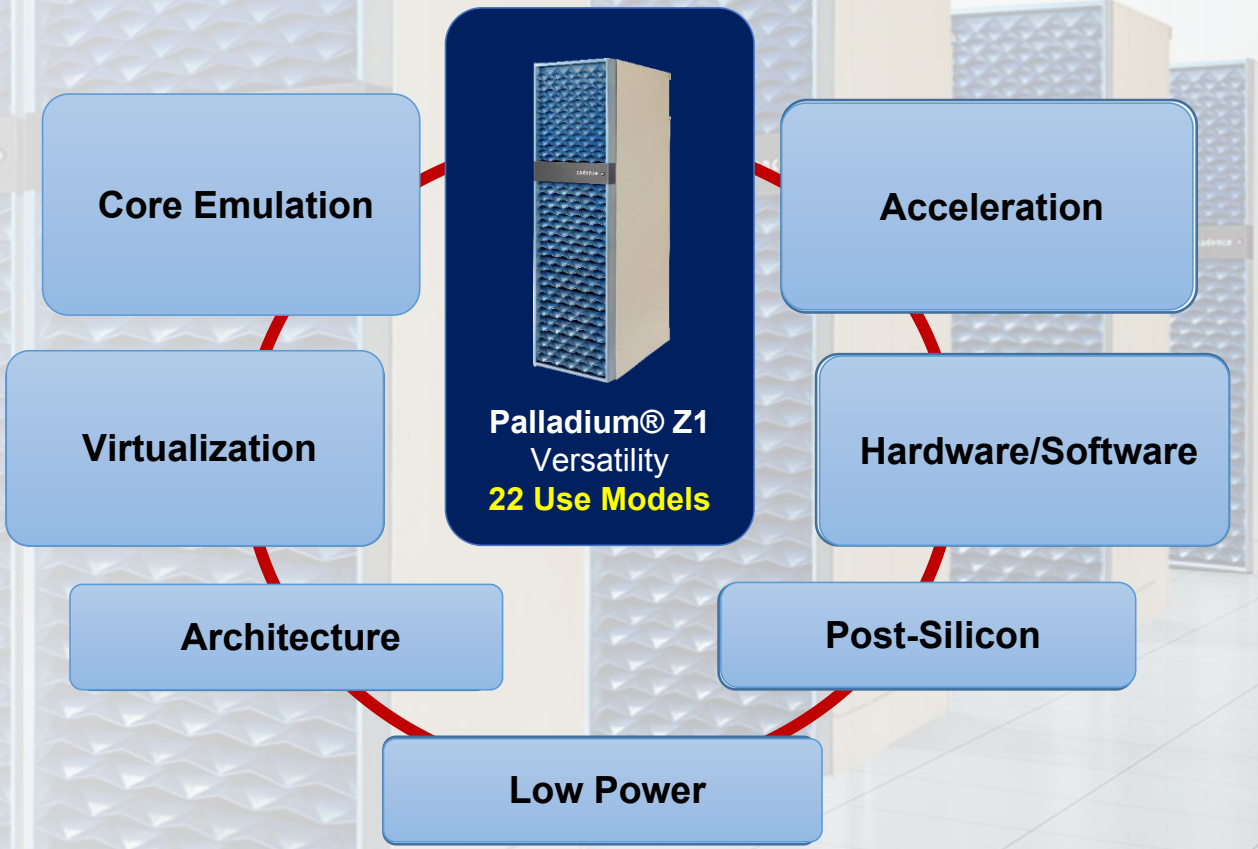
- Unified Flow
  - Reuse of the existing Palladium environment (clocks, memory models, scripts, AVIPs, SB/EDK, etc.)
  - Congruency between emulation and prototyping
  - Going back to emulation for detailed debug

Palladium Z1 Emulation Drivers

Multi-Project Use – Emulation Farms



Multi-Use-Model Versatility



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Palladium Z1 key characteristics

- Scalable datacenter-class emulation system
  - IP to full SoC emulation: 4 to 576 million per rack
  - Scales up to 9.2BG with up to 2,304 parallel jobs
  - Rack-based form factor: setup in existing data center
  - Built-in redundancy for reliability

- Virtualization
  - Virtual target relocation
  - Advanced job reshaping
  - Emulation Development Kits (EDK)
  - Virtual Emulation and Virtual Debug

4 to 576MG
User capacity

1152 GBytes
User memory

1152 GBytes
Debug memory

Up to 56 Gbps
Infiniband, per port

Up to 4MHz
Max perf.

Up to 140MG per hour
Netlist compile

13,824 IOs
(4608 per cluster)

Palladium Use Modes

Simulation Acceleration, Virtual and In-Circuit Emulation

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Simulation Acceleration

TB-driven HW verification

Test Environment

Simulator

Test-Bench
UVM-A, C/C++

Virtual Emulation

SW-driven HW verification
Interface-driven HW verification
HW/SW co-verification

Test Environment

Virtual Device Models

Application / Tester

Virtual Interfaces

Palladium

Embedded Device Models

Physical Interfaces

Fast Compile

FullVision Debug

Coverage Assertions

Multi-run Modes

Low-power DPA

In-Circuit Emulation (ICE)

SW-driven HW verification
Interface-driven HW verification
HW/SW co-verification

Test Environment

Physical Devices

Application / Tester

Faster Compiles Resulting in Higher Productivity

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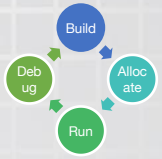
IXCOM Modular Compiler, VXE21.02

Fclk 424KHz

Compile time 5:42:08

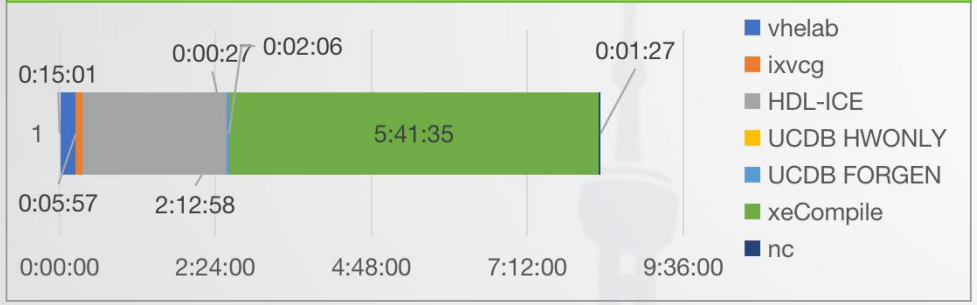
71% faster compile

- Workstation: PD02, 96-core, 2TByte
- MC workstations: Machine farm through LSF, 1TByte



IXCOM Parallel Partition Compiler VXE 19.10

Fclk 541KHz



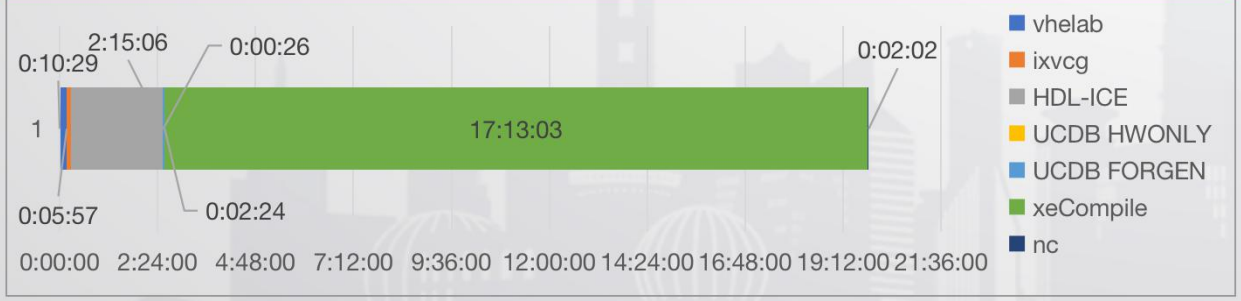
Compile time 8:19:31

57% faster compile

- Main workstation: PD02, 96-core, 2TByte
- PPC workstation: PD03, 72-core, 3 TByte Running 18 partitions on PPC workstation

IXCOM standard compile VXE 19.10

Fclk 786KHz



Compile time 19:47:25

- Workstation: PD02, 96-core, 2TByte

- Z1 configuration: 8-clusters

Palladium Debug

Unparalleled levels of productivity and at speed

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FullVision View any design signal at full speed. Debug design

Dynamic Probe Capture select signals with large traces (up to 80M samples).

InfiniTrace Capture extremely long trace depth for post-analysis replay, move forward & backward to debug any time window of interest

Offline Debug Offline concurrent debugging on workstation. Free up Palladium resource for other jobs, jump to any time window using a specific trigger

Waveform streaming Continuously view small number of signals at full rate

Save/Restore Re-start emulation run from a previous state. Save time by restoring, avoid repetitive initializations or sequences

Hot-swap Swap state of design back to simulator for interactive debugging to free up Palladium resources for non-interactive jobs

Force Change design function during runtime. Set system conditions to analyze design behavior under un-modeled corner cases

SDL/DRTL Specify multi-level complex trigger conditions. Use design events to detect scenarios,

Control

Determine **when** to
- Capture signals
- Stop emulator
- Log messages

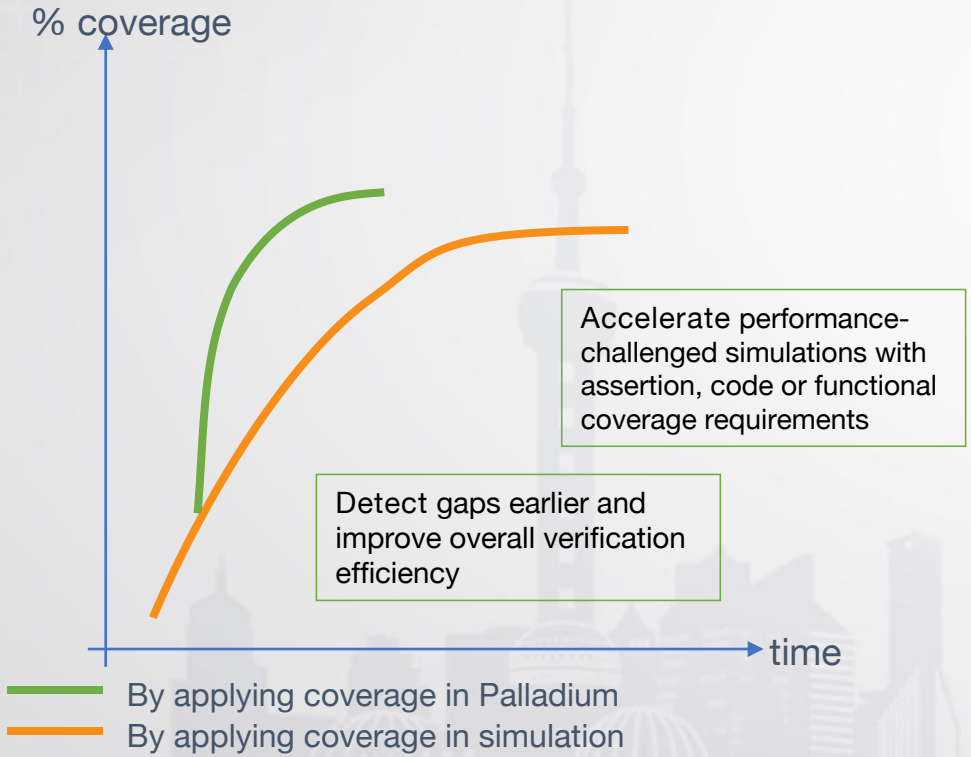
Visibility

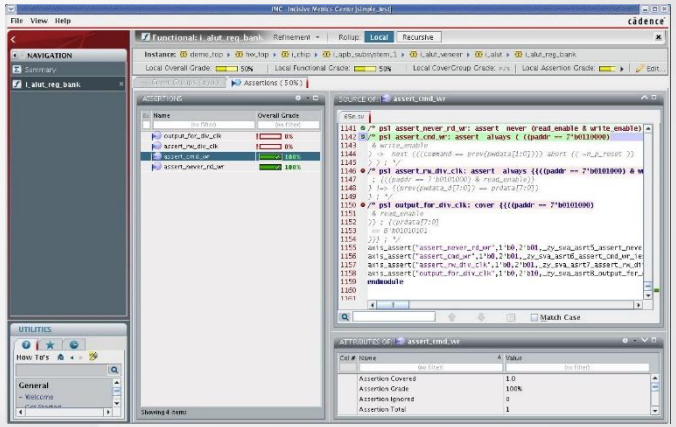
Determine **what**
- Signals to capture
- Debug technology to apply

Combine control & visibility
- Triggering waveform capture
- Full Vision & Waveform streaming
- Compiled Monitors with dynamic technologies (DRTL and SDL)

Palladium coverage support

- Palladium supports assertions, code and functional coverage
  - Scored in hardware & viewed in software
  - Supports acceleration & in-circuit emulation





Visualize coverage in
Xcelium Metric Center (IMC) or vManager

Protium X1 Enterprise Prototyping System

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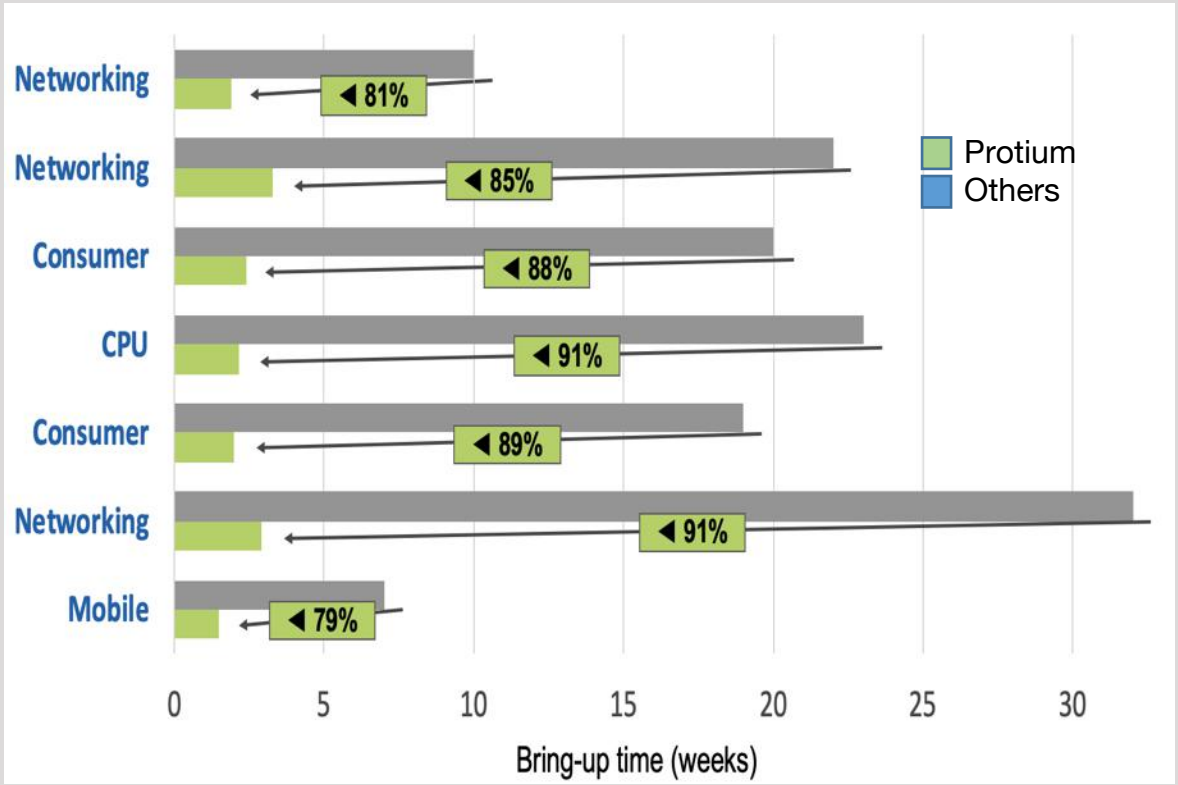
- Performance
  - Enabling early firmware and software development, automated bring-up
  - Up to 50MHz for single FPGA; up to 5MHz on billion gate designs
- Capacity
  - Advanced blade architecture scales to billions of gates
  - Ideal for AI, ML, 5G, mobile, and graphics applications
- Fast Bring-up
  - Unified Palladium® Z1 / Protium™ X1 compile ensures DUT congruency
  - Enables transition from emulation to prototyping in days
- Multi-user
  - Single-FPGA granularity assures high utilization and efficiency
  - Ideal for storage, automotive, image, consumer and medical applications

Technology Details – Faster Prototype Bring-up

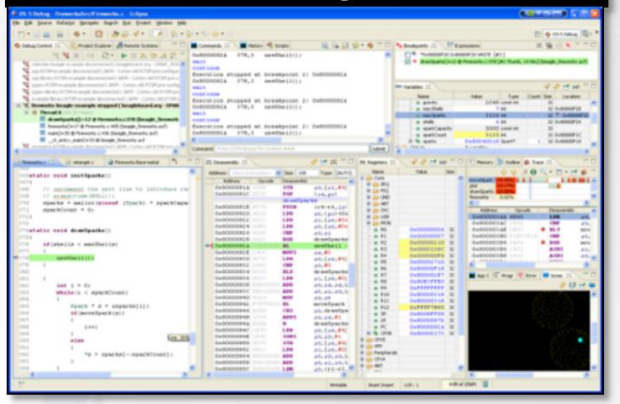


- Unified compile
  - With Palladium® Z1, Protium™ S1
  - Bring-up in days or weeks (vs. months)
  - Re-use of existing environments
  - Easy transition from emulation to prototyping
- Enhanced memory modeling
  - Map virtually any design memory
  - New: LPDDR5, UFS 3.0 and HBM
  - Future protocols can be added quickly
- SpeedBridge® Adapters
  - Connect to peripherals quickly
  - Without manual rate-adaption

Technology Details – Advanced Debug Capabilities

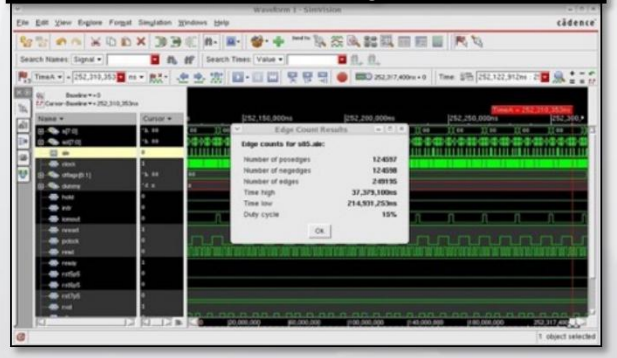
- Hardware debug: bring-up design quickly, validate functionality
  - Force and release: for initialization and “what-if” analysis
  - Data capture card (DCC): 1000’s of signals, millions of cycles
  - Prototyping Full Visibility: observe any signal at any time

Software Debug: C Code



- Software debug: early firmware and software development
  - Memory (backdoor) upload and download
  - Clock control to stop and resume the hardware at any time
- Standard interfaces to industry-leading debuggers and software environments - use familiar tools
  - Joint Test Action Group (JTAG) and Universal Asynchronous Receiver/Transmitter (UART) interfaces
- Transaction interface
  - Directly connect to software models and virtual environments

Hardware Debug: RTL

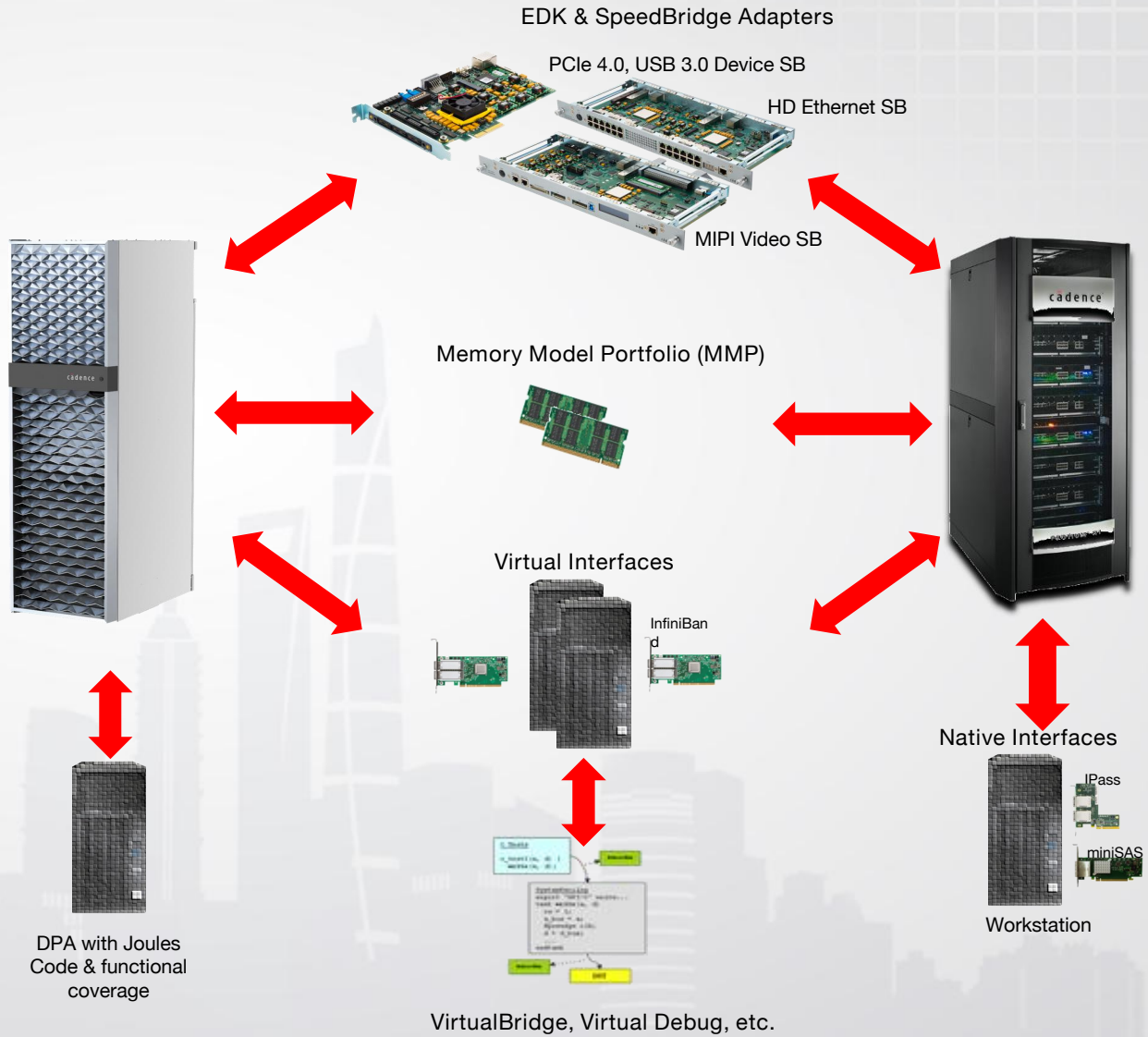


Technology Details – Multi-user Functionality

- Prototyping of smaller IP or subsystems
- Flexible multi-user capability for up to 6 concurrent users per blade
  - Any single-FPGA granularity combination is possible – no restrictions
  - "Cloning" of design is supported (same design in multiple FPGAs) without recompile
- Enables optimal utilization for IP, IoT, storage, automotive, image, consumer and medical designs

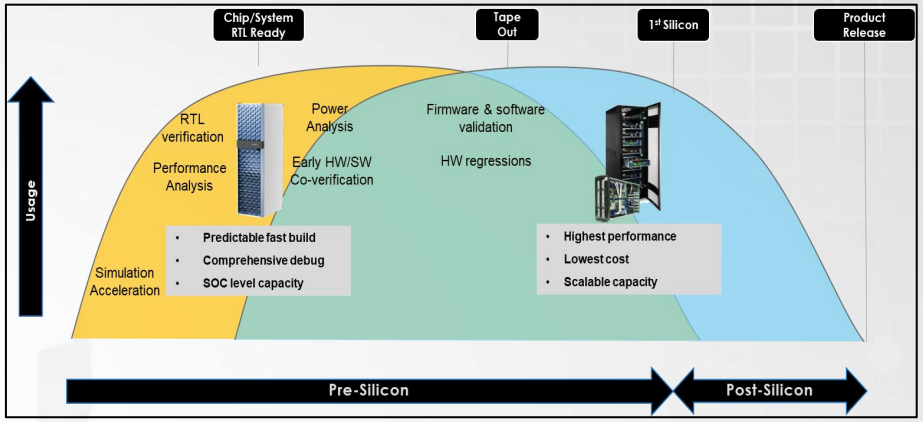
Shared solutions and peripherals

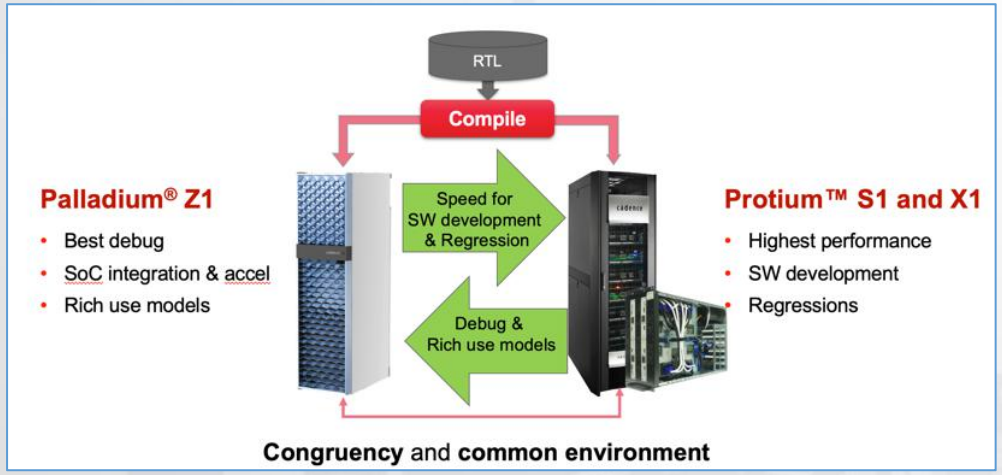
- EDKs and SpeedBridge Adapters
  - Physical connection to real-world interfaces
- Virtual Solutions
  - VirtualBridge, AVIP, Hybrid, Virtual Debug
  - InfiniBand-based link to virtual interfaces
- Memory Model Portfolio (MMP)
  - For all on-chip and off-chip memories
- Job Scheduler and vManager
  - Manages workloads across Z1/X1 platforms
- Palladium only
  - Dynamic Power Analysis with Joules
  - Code and functional coverage
- Protium only: native interfaces
  - Highest throughput
  - “breaks” congruency



A Common Methodology Makes Life Easier

- Unified Flow
  - Reuse of the existing Palladium environment (clocks, memory models, scripts, AVIPs, SB/EDK, etc.)
  - Congruency between emulation and prototyping
  - Going back to emulation for detailed debug





- Common Compile Front-end
  - No learning of new tools and flows
  - Identical language coverage
  - New capabilities and fixes available on both platform simultaneously

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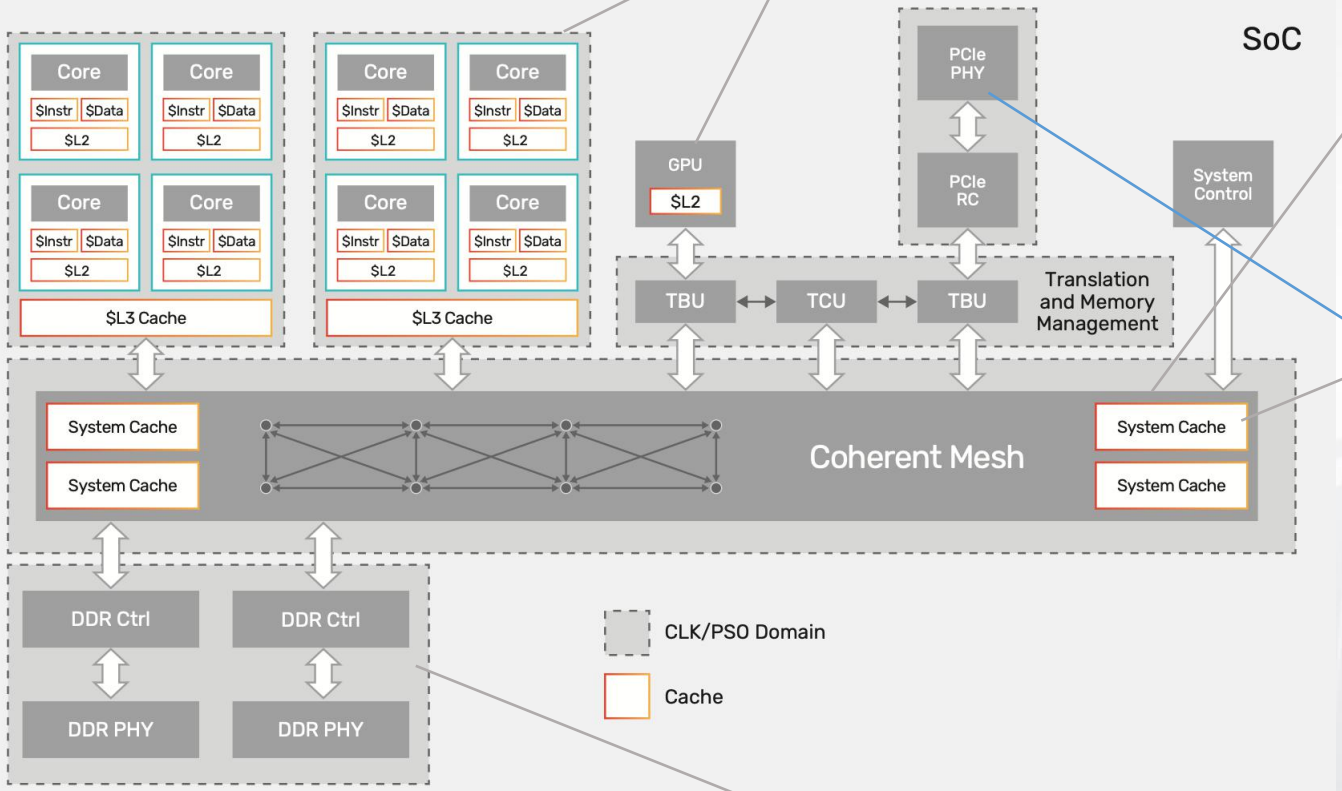
Accelerate SoC Performance Testing with System VIP

Why Is SoC Performance Testing a Growing Challenge?

Number and variety of processing engines is growing to address More than Moore



SoC Infrastructure has become a mass of coherent and non-coherent interconnects stitched together with clock and domain bridges to support multiple power domains.

To maintain growing demands for SoC performance the number of cache hierarchies is growing with each generation. Combined with high-speed coherent I/O creating complex scenarios and measuring results is tough

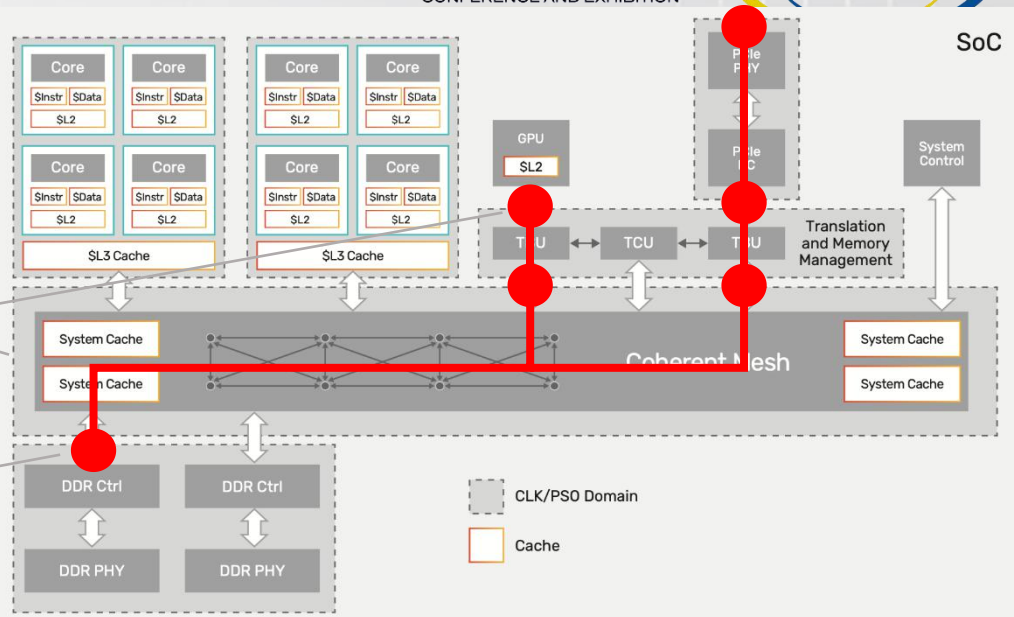
To keep pace with system throughput demands, DDR subsystems are becoming more complex, multiple controllers allied to complex hashing in the controllers and interconnects to ensure balanced DDR loading

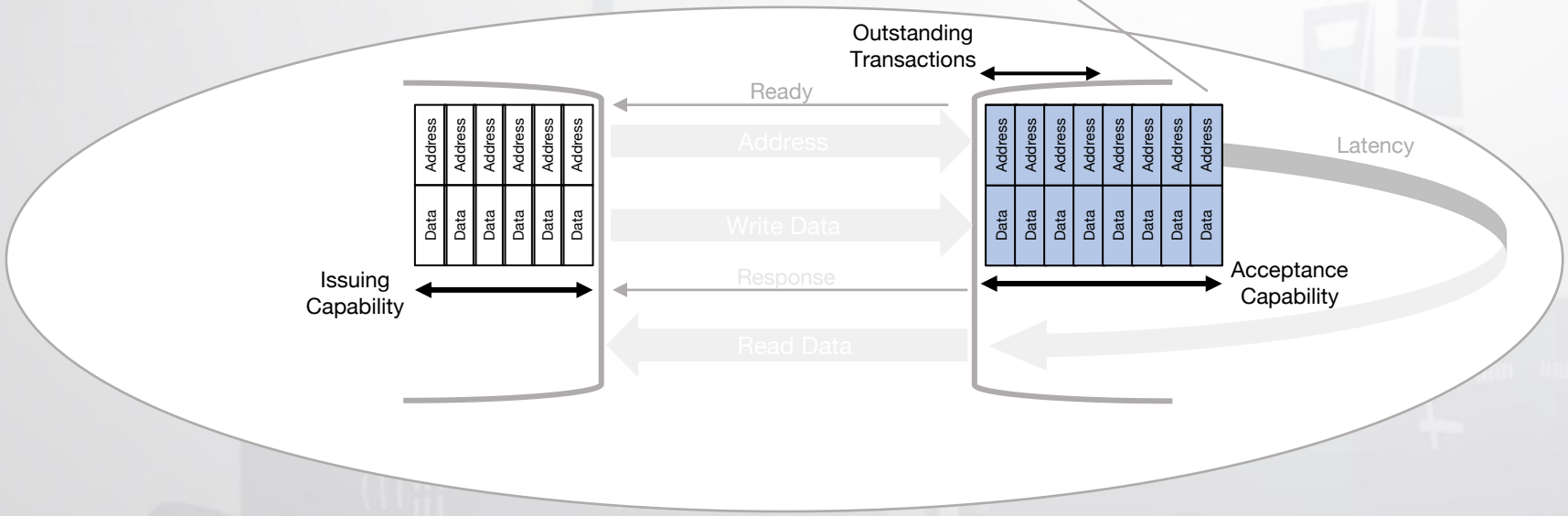
Understanding Performance Throttling

Quality of Service (QoS) settings can adjust priorities when the system becomes more highly loaded.

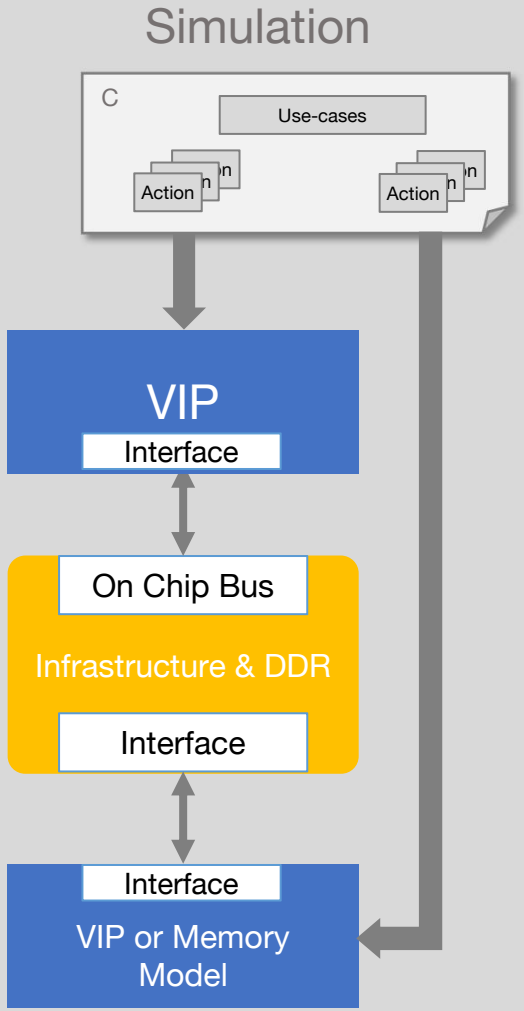
If the situation persists it can cause back-pressure to build all the way back to one or more Initiators

Once a Responder cannot keep up with demand, it creates “back-pressure”





A Systematic Approach to Ensuring SoC Performance

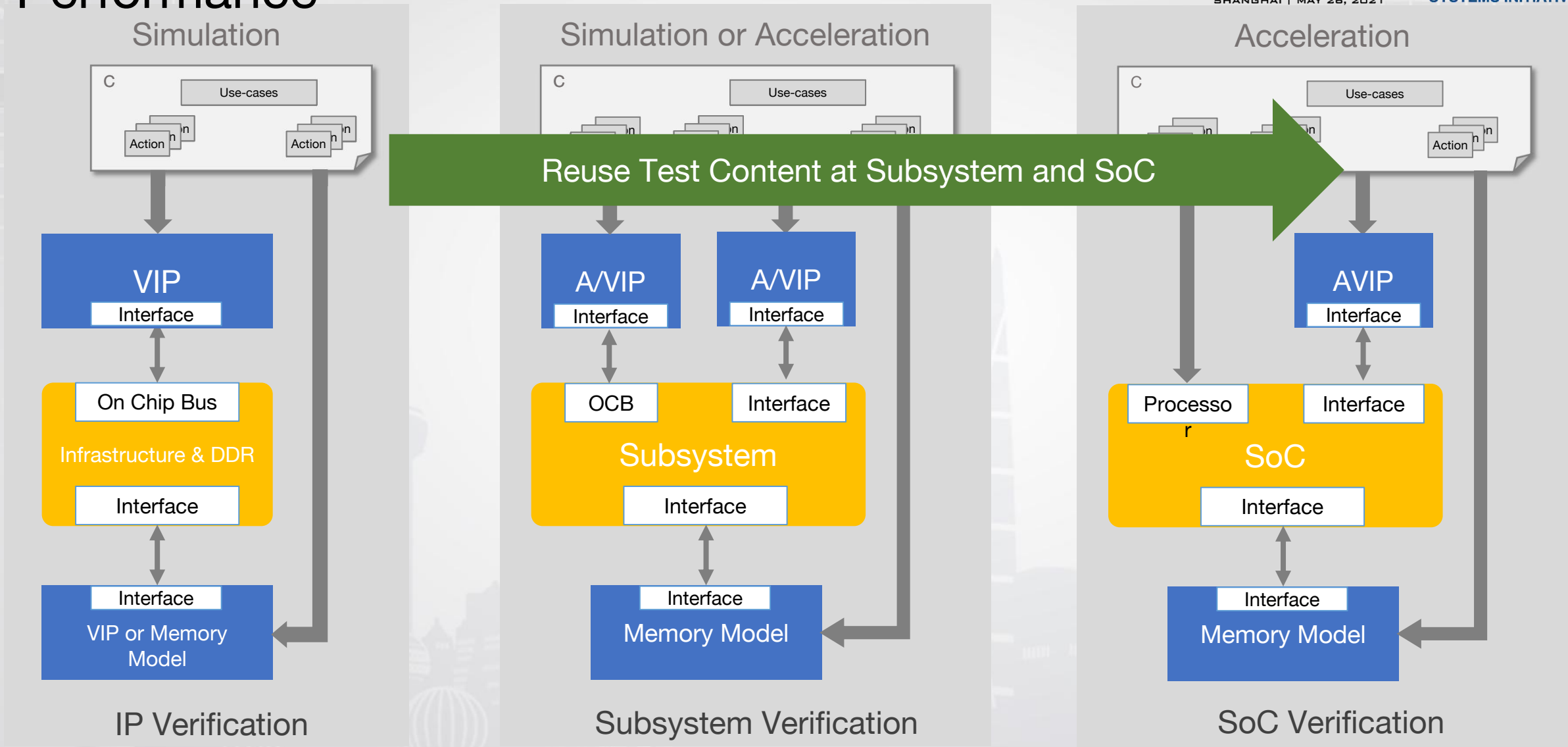


Step 1 – Characterization
- Path-by-path maxBandwidth, minLatency analysis
- Sweep Outstanding Transactions to find sweet spot

Step 2 – Synthetic Workloads
- Traffic Generators for non-coherent scenarios
- Basic Coherency Tests – cache hit rate sweeps
- Advanced Coherency Tests – complex multi master scenarios

Step 3 – Sign-off
- Define sign-off performance scenarios
- Create sign-off checks
  - Self-checking scenarios
  - Post-processing performance checks

A Systematic Approach to Ensuring SoC Performance



How Does System VIP Help?

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Generation and Stimulus

Analysis and Checking

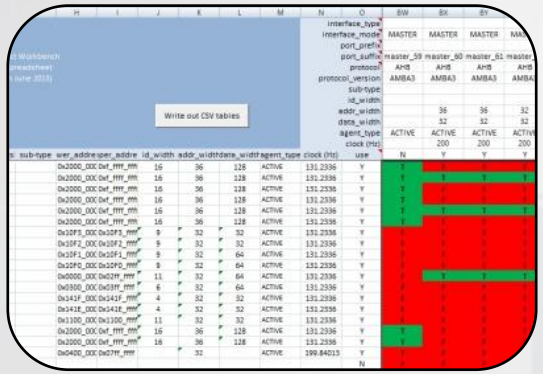
Testbench Assembly

SoC Test libraries

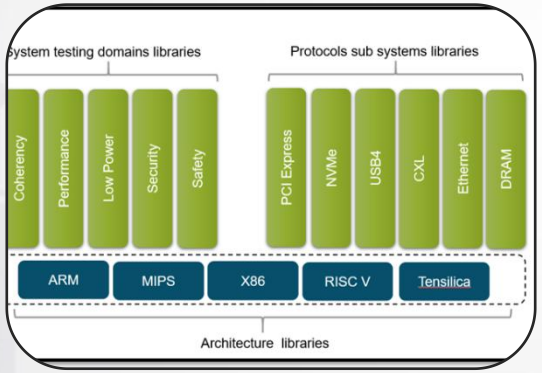
Cadence® System VIP

SoC Performance analysis

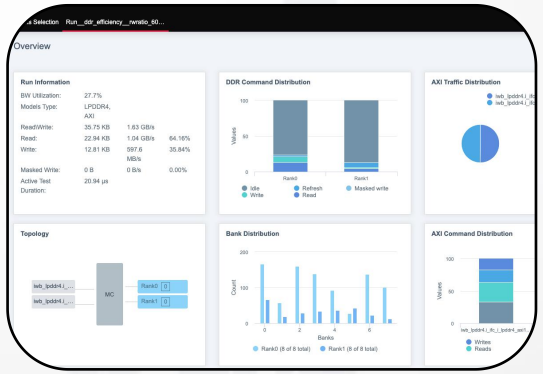
Data / Cache coherency checkers



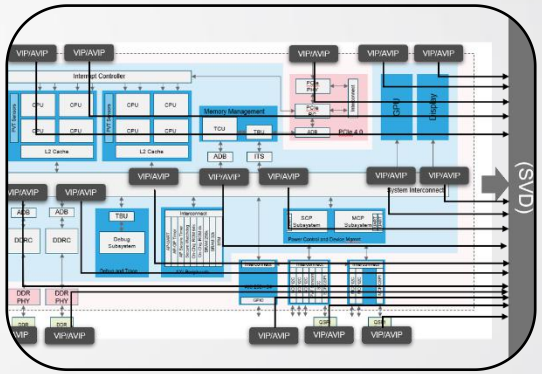
System Testbench Generator



System Traffic Libraries



System Performance Analyzer



System Verification Scoreboard

RISC-V®

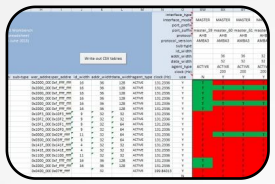
arm

x86

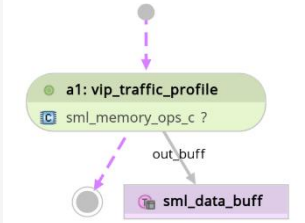
What Does an Automated SoC Performance Flow Look Like?

Flow

1. Generate Testbench
   - Configure CSV for Simulation
   - Generate SV UVM or C testbench
2. Scenario Creation
   - Initialization of DUT
   - Basic ATP Test
   - Basic Coherency Tests
   - Advanced Coherency Tests
3. Run Tests
   - Simulation or Acceleration
4. Analyze and Debug
   - SPA Performance Analysis
   - SVD Correlation



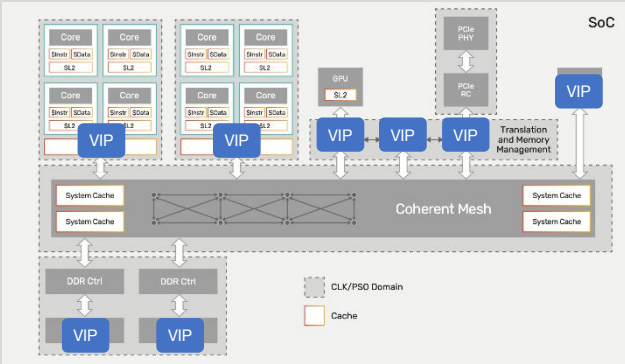
csv data



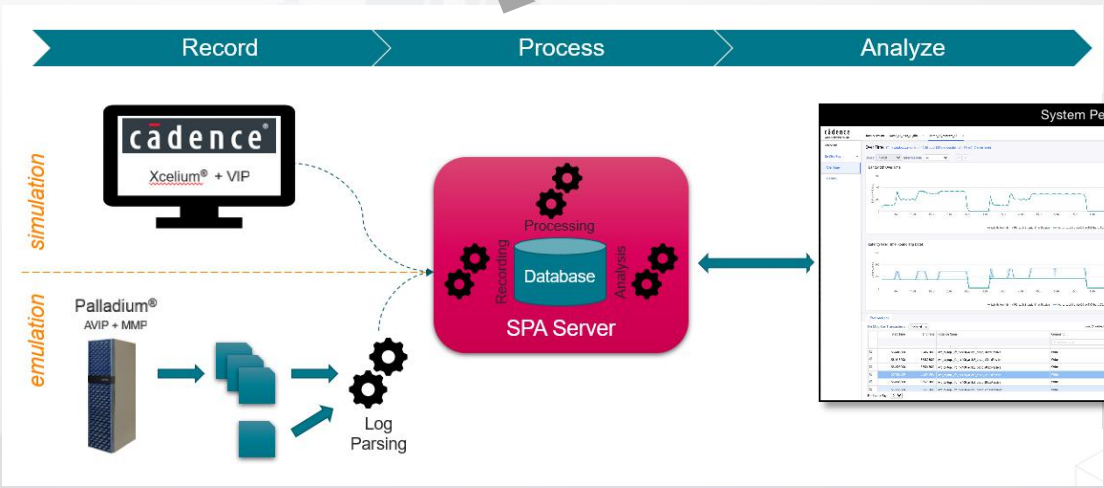
Traffic Libraries

System Testbench Generator

Perspec™

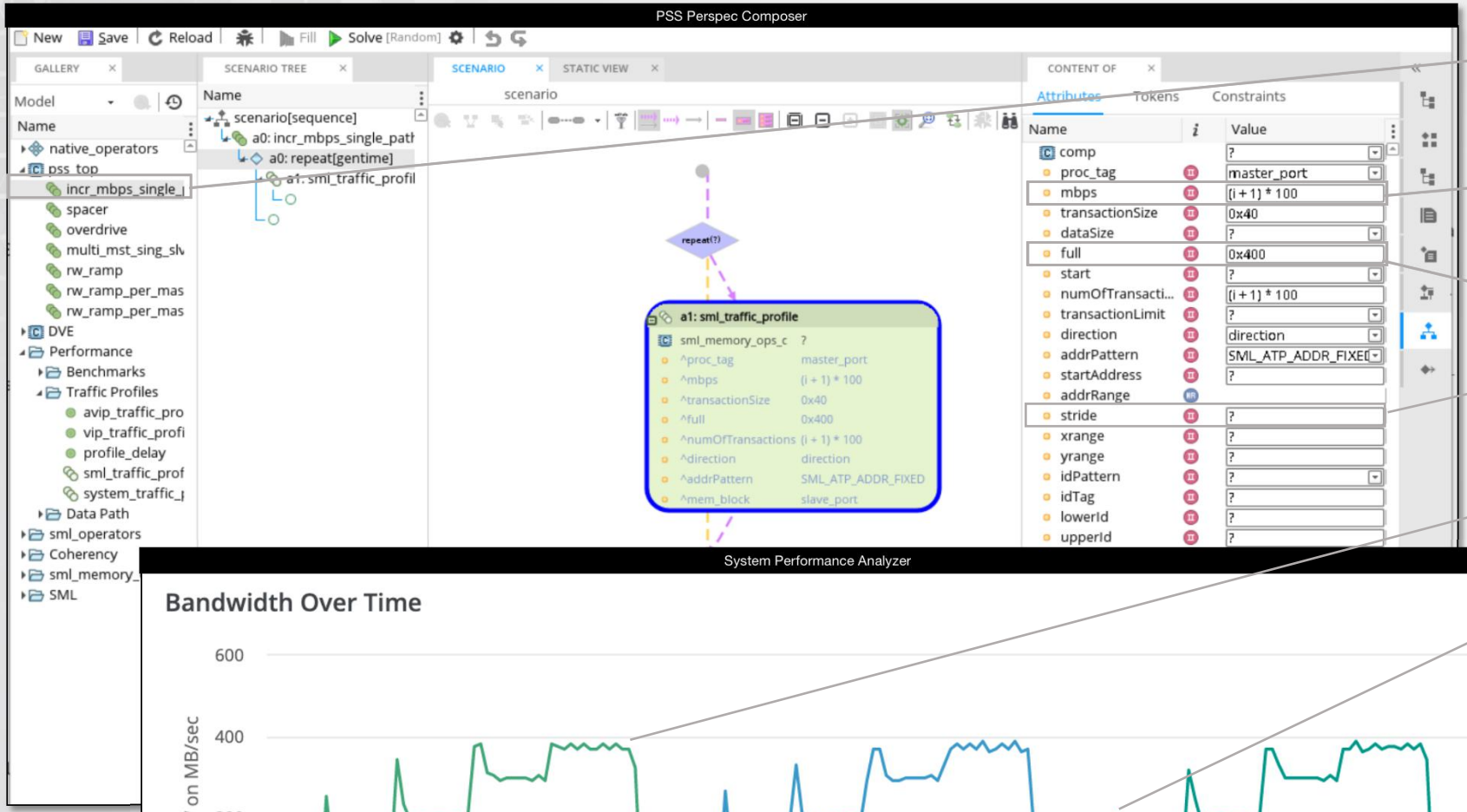


Portable Performance Scenarios



What Does an Automated SoC Performance Flow Look Like?

Scenario creation



Drag and drop ”Actions” from the gallery which shows libraries and user code :- Increment Bandwidth from 100MBs to 400MBs

Fields can have fixed values or in this case in a repeat loop to create 4 sequential ATP Actions

ATP FIFO Configuration models bursty IP behaviour

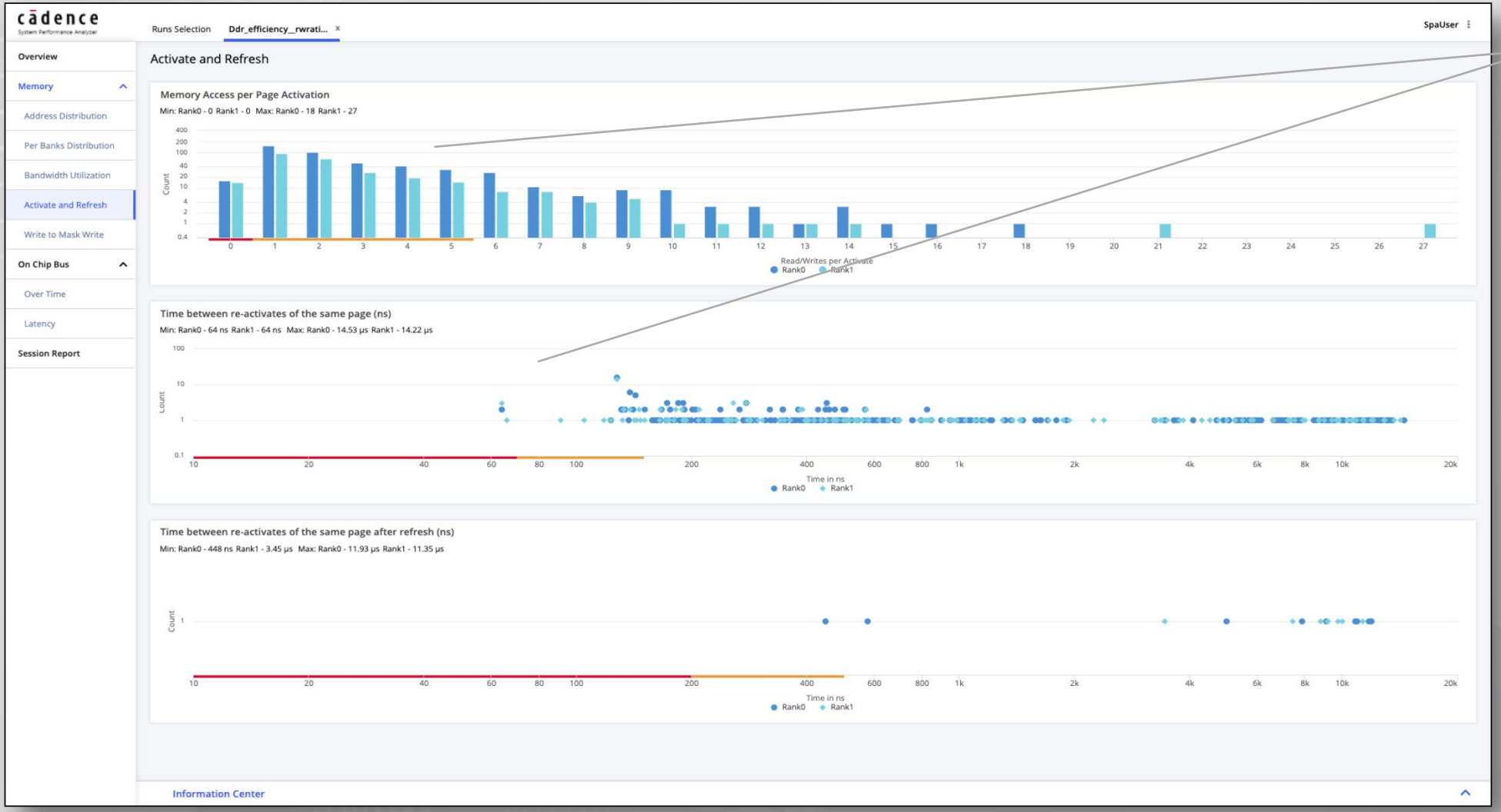
Fields with a “?” indicate that the Solver will generate a random value unless the user overrides with a contrained value.

400MBs is the max possible on this interface, therefore there is some minor throttling going on

FIFO creates the initial ”burst” of transactions which has a bigger effect at lower bandwidths

What Does an Automated SoC Performance Flow Look Like?

DDR analysis



The DDR analysis tools help identify potential areas of concern for DDR performance

What Does an Automated SoC Performance Flow Look Like?

Debug – Root causing problematic transactions

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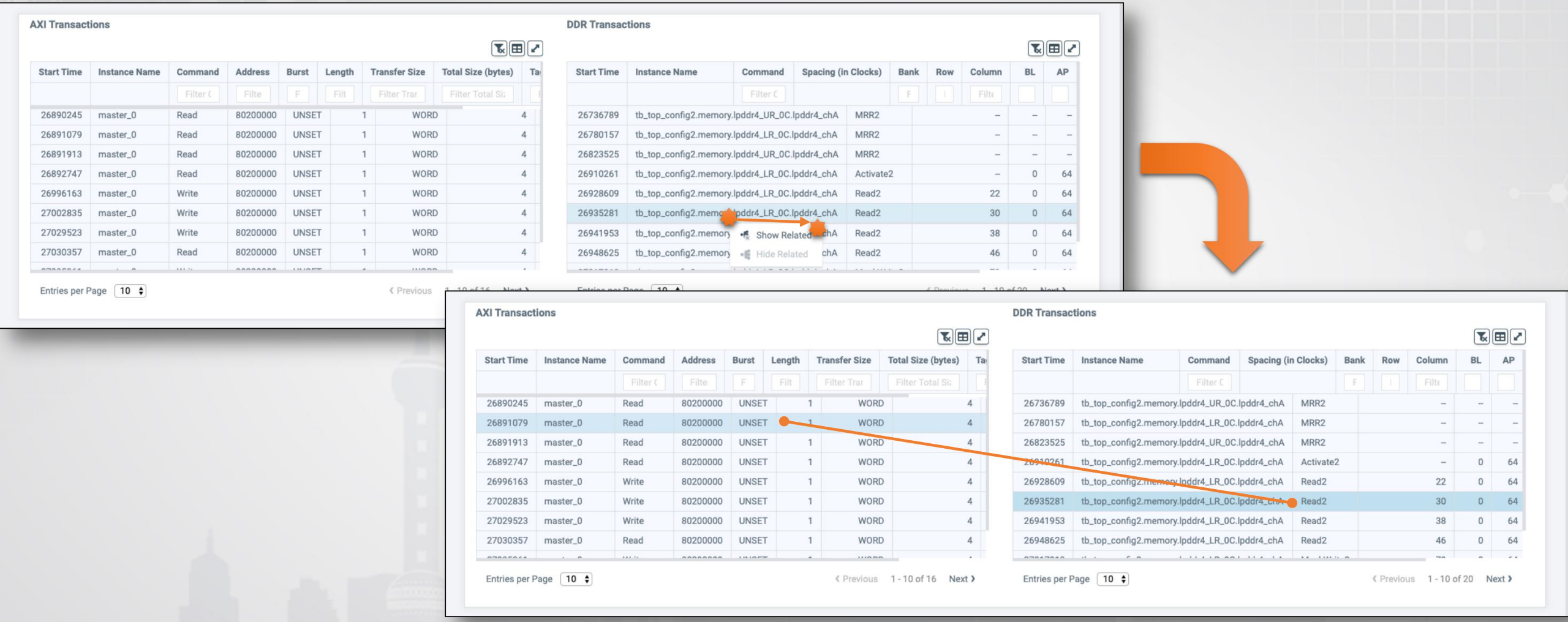

Cadence System VIP

Automate and speed up SoC level verification with pre-define content and tools

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Cadence®
System-Level Verification IP

Chip-level test and testbench generation with advanced analytics

System Testbench Generator

- UVM SV testbench for simulation
- C testbench for emulation

System Traffic Libraries

- Cache coherency, performance, PCIe®
- Seamlessly in sim, emulation, and silicon

System Performance Analyzer

- Memory, interconnect, and peripherals
- Unified for simulation and emulation

System Verification Scoreboard

- Checks data and cache coherency
- Supports simulation and emulation

> Renesas has used Cadence VIP for many years and values Cadence's leadership in advanced SoC verification technologies. By adding the new System VIP to our existing verification environment based on the Cadence Xcelium and Palladium platforms, and improving stimulus re-use and automation, we've further accelerated the SoC verification process with **10X more efficiency**, enabling us to deliver innovative, high-quality products to our customers faster.

Tetsuya Asano
Director, Design Methodology Department, Shared R&D EDA Division at Renesas Electronics Corporation

RENESAS

> Through our collaboration with Cadence, we've reduced some of the complex SoC verification challenges, especially around I/O peripherals. By using Cadence System Traffic Libraries and System Performance Analyzers, Arm was able to automate complex test generation processes, enabling a quicker PCIe integration verification and performance analysis.

Tran Nguyen
Director of Design Services at Arm

arm

Summary

- Ensuring SoC performance targets are met is a growing challenge
  - Bigger testbenches, multiple runtime engines
  - Building richer scenarios
  - Harder to analyze and debug
- Testbench automation is essential to be productive
- Building all the required scenarios is becoming a large task
  - Reuse of the scenario content is essential
  - Easy porting of content to different SoCs and execution engines is a must
- Analyzing and debugging performance requires domain-specific tools
  - On-chip bus, DDR, and other domains need special analytics
  - Tracing the transaction lifecycle across an SoC is extremely challenging without tools

System VIP addresses the challenges

Cadence Verification Solution

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Find and fix the most bugs per $ compute per day

Smartest Apps

Smart Verification Management
vManager™ – Indago™ – VIP – System VIP – Perspec™

Fastest Engines

Formal	Simulation	Emulation	Prototyping
JasperGold ™	Xcelium™	Palladium™	Protium®
			

Most Choice of Compute

X86 or Arm® CPU	X86 or Arm CPU	Custom Processor	FPGA

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THANK YOU

Vielen Dank

Obrigado!

Gracias

धन्यवाद

Merci