



SYNOPSYS®

PCIe Gen5 Validation—The Real World



Agenda





- What are challenges with PCIe validation?
- HAPS-100 New Generation Prototyping platform
- Case Study 32 Gbps PCIe Gen 5 validation with HAPS-SX/HAPS-100 1F (VU19P)
- Fast validation bring-up: Speed adaptors for HAPS

HAPS Portfolio to Serve All Markets Industry's Fastest Prototyping Solution





HAPS-SX



Range of FPGAs

HAPS HW products

HAPS-80



Largest ecosystem worldwide

Integrated prototyping solution

HAPS-100



Adopted by Market Leaders

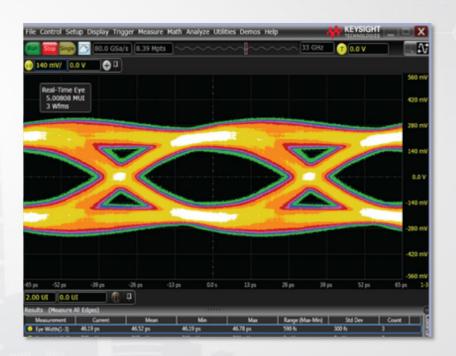
Advancing prototyping leadership

Challenges with PCIe Gen 5 Validation





- 32GT/s data rate and double link bandwidth from 64GB/s to 128GB/s
- Additional challenges with the PHY design
 - For prototyping validation an external PHY card is needed
 - Special requirements for connectors, cables, clocking, jitter and routing
- Xilinx UltraScale+ with VU19P does not support a PCIe Gen5 PHY
 - Special testing of the FPGA to Achieve 32GT/s









Industry's highest performance prototyping system

Addresses Key Challenges in Prototyping

Fastest Single FPGA Desktop System

Multiple speed-grades; Highest possible transceiver speeds Ideal for high-performance IP such as PCIe, USB

Rich Connectivity for Daughercards

25 HT3 connectors (24 HPIO, 1 HDIO); 6 Quads transveiver connectors (MGB2A); Compatible with HT3 and MGB daughter cards

Flexible Interfaces

One QSFP host connection and one USB3 host connection; Built-in Mictor38 and UART interfaces; 4*6 clock outputs and 4*6 clock inputs; 18 clocks on the user-FPGA

> IP Debug Flow feeding into Verdi Built-In 8 GB DDR4 memory for Debug

New-generation Prototyping Architecture

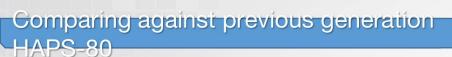
Advancing Prototyping Technology Leadership



Supports HAPS
Daughterboard Ecosystem



Advancing Prototyping Technology Leadership





- 1.5x performance
- 50% more FPGA IO
- MGTDM: 10+ MHz at 1024:1 ratio

Capacity

- 1.6x Capacity increase
- Scales to large setups, up to 64+ cascading
- Multi User Mode

Debug

- 4x performance and 4x increased sample depth
- Improved performance for multi-FPGA Global State Visibility





- Clocks
 - 48 global clocks (24 PLL-Generated, 24 via Clk-In Ports)
- Host Interfaces
 - Up to 10x increase in host interface bandwidth
 - Two QSFP & one USB3 interface vs one USB2
 - Support for UMRBus3
 - High flexibility for Clocking, Debug, Host Interface





HAPS-100 Prototyping SW for High Performance

HAPS-100 Capabilities	HAPS-100 Prototyping SW
Front-end compile	Unified Compile with VCS
Partitioning	Automated, architecture aware
Memories	Automatically inferred
Incremental compile	Distributed
Debug signal capture	On-chip memory, Deep Trace Buffers, Global State Visibility
Waveform debug	Unified debug with Verdi
Hybrid	Supported
Gated clock conversion	Supported
DesignWare Foundation IP	Supported
Cross Module References	Supported
Power validation (UPF)	Supported
FPGA P&R	Customized Xilinx Vivado included
	HAPS-100

HAPS-100

HAPS-100 Provides High Performance



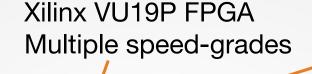


25 HT3 Connectors

2 Host Ports 1xUSB3 1xQSFP28

6 Quad Transceivers (MGB2)

USB-to-JTAG / UART USB-to-Quad UART

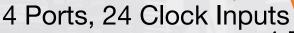


Mictor38 connector

8 GByte Debug Buffer

Desktop / Benchtop friendly architecture

Proven, Reliable High-Speed Cables
Improved Cable Connectors against bent p
Build-in Diagnostics



4 Ports, 24 Clock Outputs





HAPS Gateway Maximizing HAPS ROI Through Resource Management

Enables access from Web browser and Pythonscripts

HAPS Lab Engineers

Ease hardware bring-up via interactive setup validation

HAPS Prototypers

Reduce support effort by delivering fully packaged prototypes

HAPS End Users

Use prototypes fully scripted or from convenience of a web browser

Infrastructure Managers

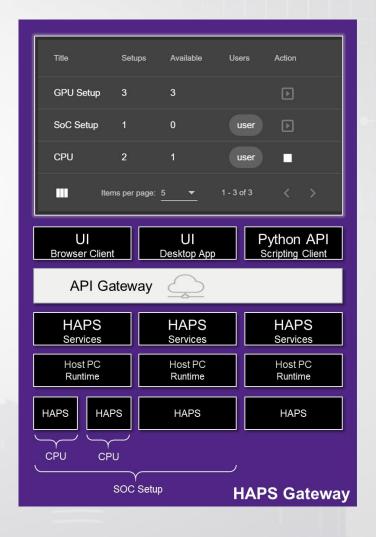
Plugs into IT (Jenkins, GitLab, LDAP, Database Server, Certificates)

Decision Makers

· Report utilization for investment planning











Case Study: PCIe Gen 5 – 32 Gbps

HAPS-SX VU19P PCIe Gen5 IP PCIe Gen 5 Prototyping Project



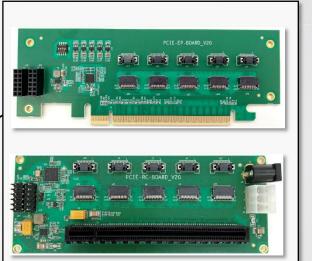


Hardware Platform

- HAPS-SX VU19P 32G with specially qualified VU19P
 - FPGA qualified by Xilinx for 32Gbps GTY line rate
 - Limited PCIe Gen 5 prototyping feasible using RTL soft IP
- HAPS Connect Partner (HCP) interface boards for PCIe Gen 5 EP ar
 - Support side band signals and GT reference clock
 - Tested for data rate of 32Gbps

Synopsys RTL Soft IP packages

- Transceiver test utility for GT link quality tests and hardware tuning
- GT-IP to assist PCle Gen 5 PHY and MAC implementation
 - · GTY reset sequence, control and configuration, and
 - 128/130 encoding, data frame alignment, etc.

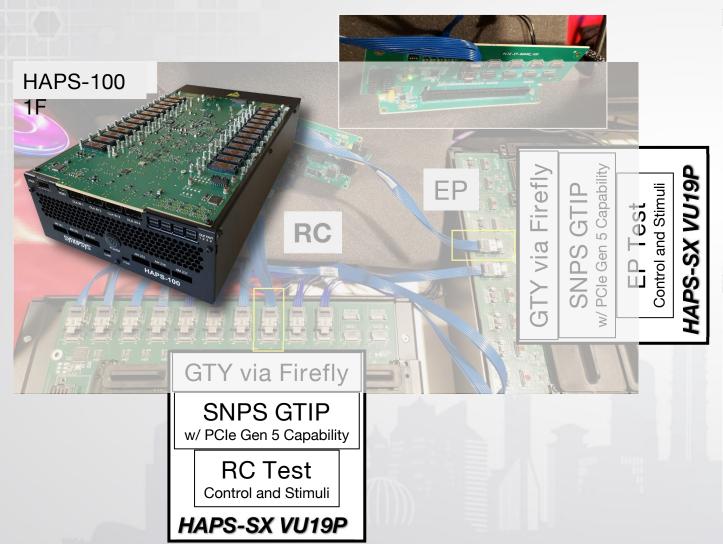


HCP PCIe Extension Cards

HAPS-SX VU19P 32Gbps for PCIe Gen 5 PCIe Gen 5 Link-up using Synopsys GTIP





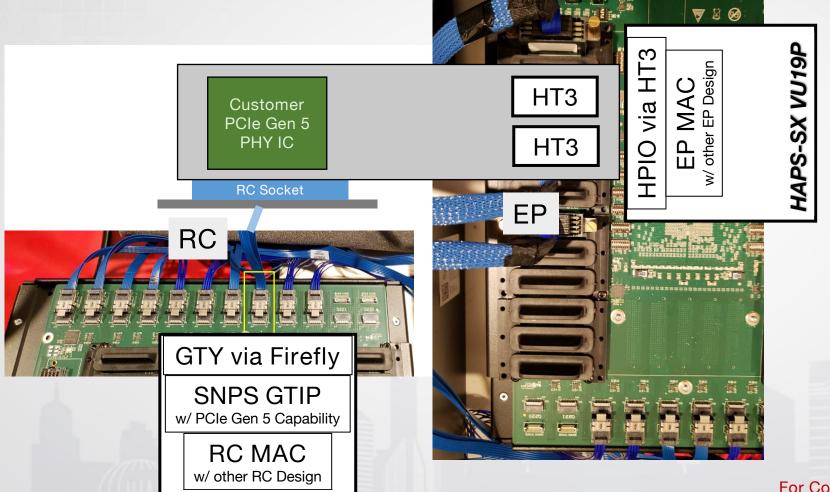












HAPS-SX VU19P

For Concept Illustration Only
Not real setup due to customer project confidentia

HAPS-SX VU19P Daughter Board Support

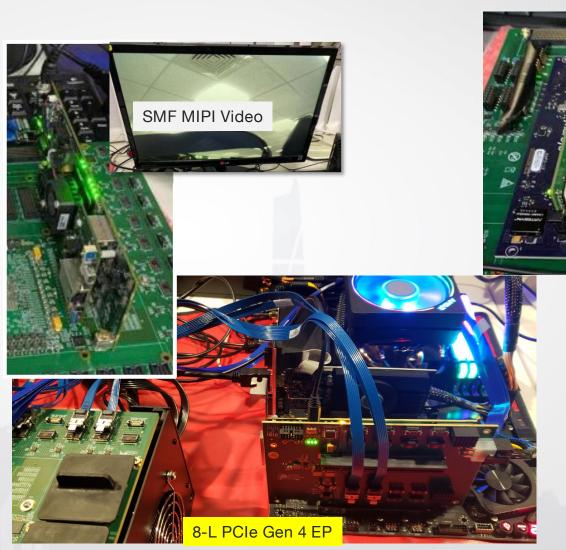




DDR4_HT3



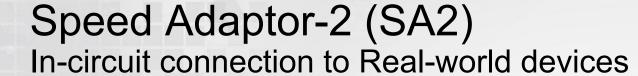








Fast Validation Bring-up: Speed Adaptors for HAPS









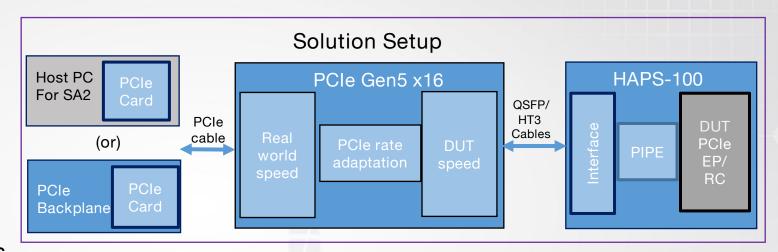
PCIe SA2 Integration





Tasks Performed

- Integrate RTL to facilitate HAPS-100
 VU19P deployment
- Integrate RTL to instantiate the hooks for the DUT to communicate with SA2
- Verified and simulation clean FPGA
 RTL
- Verified by using prototypes in the lab









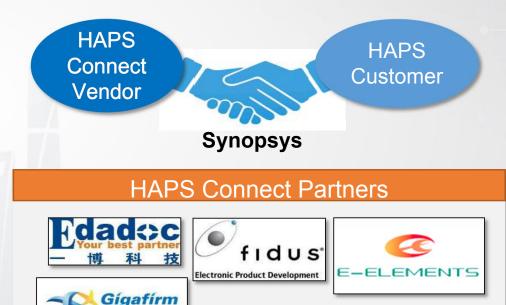
HAPS Protocol Interface Solutions





Ecosystem offering comprehensive portfolio of HAPS Extension Cards

- Protocol Interface Extension cards are essential in 90% prototyping setups
- 85+ Protocol Interface implementations supported
- Daughter board and services for HAPS systems
 - Complimentary portfolios
 - Customization
- Leverage daughter boards from leading industry vendors
- Reduce project risk
- Save prototype development costs and resources









Unified Compile with VCS

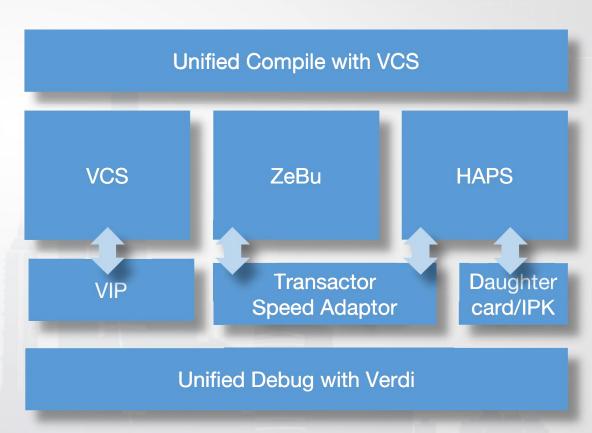
- Common language parser across simulation, emulation, prototyping, formal and debug
- SystemVerilog assertion (SVA) support via trigger conditions and waveforms
- Reuse VCS setups

Unified Debug with Verdi

- Common debug data base and use modes
- Continuum debug flows between engines

Unified Protocol Support

- Industry's largest portfolio of VIP, Transactors, Speed Adaptors, Daughtercards and
- IP Prototyping Kits (IPK)
 - · All DesignWare IP is validated on HAPS



Summary





- PCIe Gen5 protocol with 32 GTs Data rate, superior bandwidth, and special PHY and connector design introduced validation challenges for prototypers
- HAPS-100 VU19P 1F and HAPS-SX VU19P are the only Xilinx qualified prototyping solution in the market for PCIe Gen5 validation at 32Gbps line rate
- HAPS-100 VU19P 1F has the cascade capability, and can scale to big systems for PCIe Gen5 real world validation
- Speed Adaptors and HAPS Extension Cards ecosystem enables HAPS users to implement over 85 protocol interfaces for using real world payloads





Q&A





Thank You

