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SHANGHAI | MAY 26, 2021

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SYNOPSYS® Silicon to Software™

Fast Forward your Software Development with Advanced Hybrid Technologies

Xiaowei Pan, AE Manager

Synopsys China

Agenda

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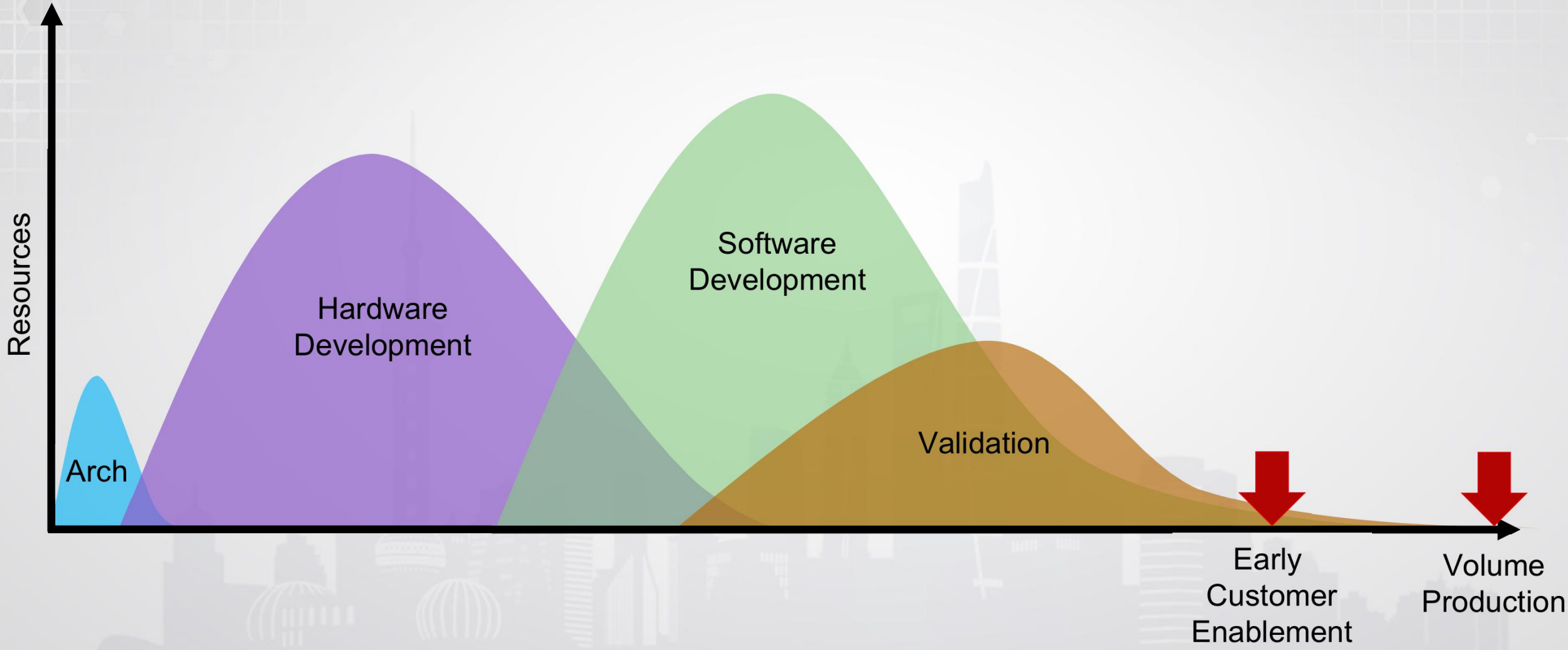
- Introduction
- Synopsys Hybrid Technologies
- Use-cases and Successes
- Synopsys Hybrid Innovation
- Conclusion
- Q&A

SoC Design Cycles are Getting Longer

Driven by Increasing Software Content and SoC Complexity



Triple Shift Left for Time-to-Market

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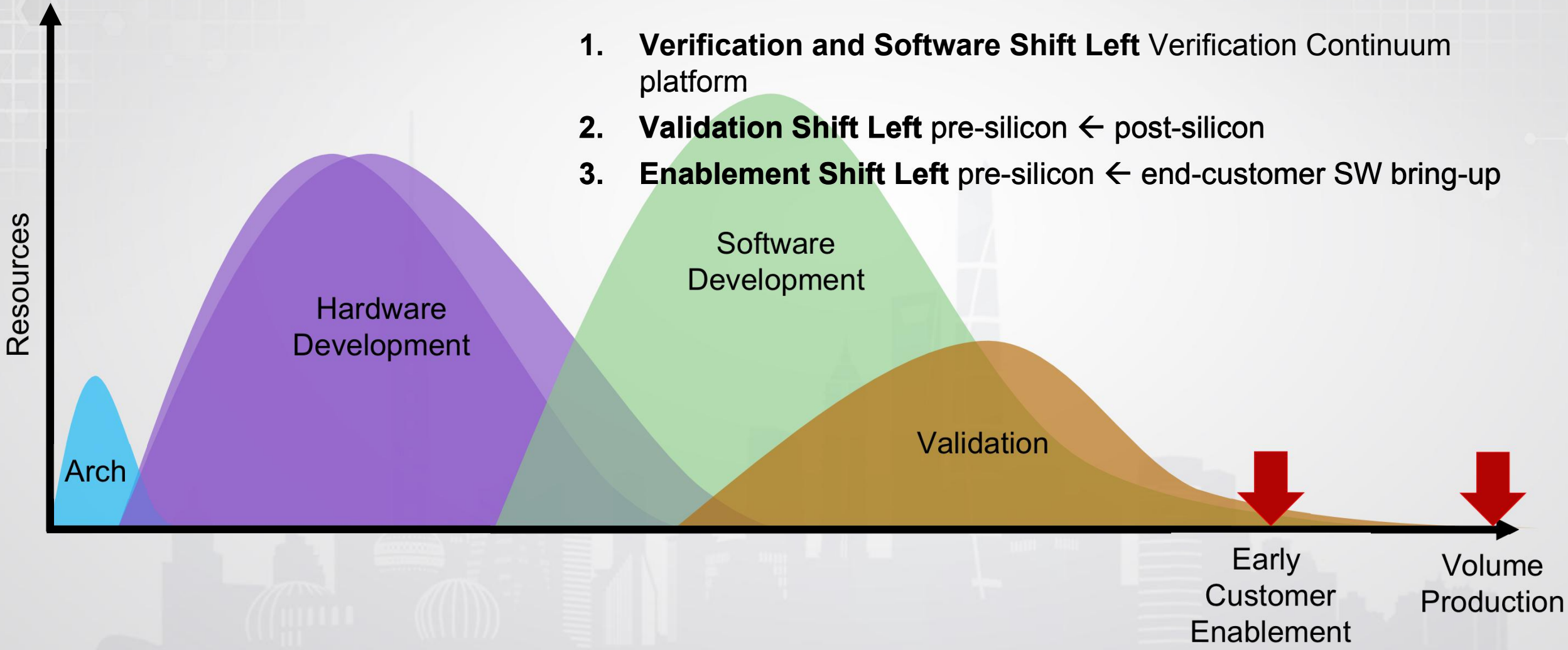
1. **Verification and Software Shift Left** Verification Continuum platform
2. **Validation Shift Left** pre-silicon ← post-silicon
3. **Enablement Shift Left** pre-silicon ← end-customer SW bring-up



How to Verify HW/SW Systems Faster?

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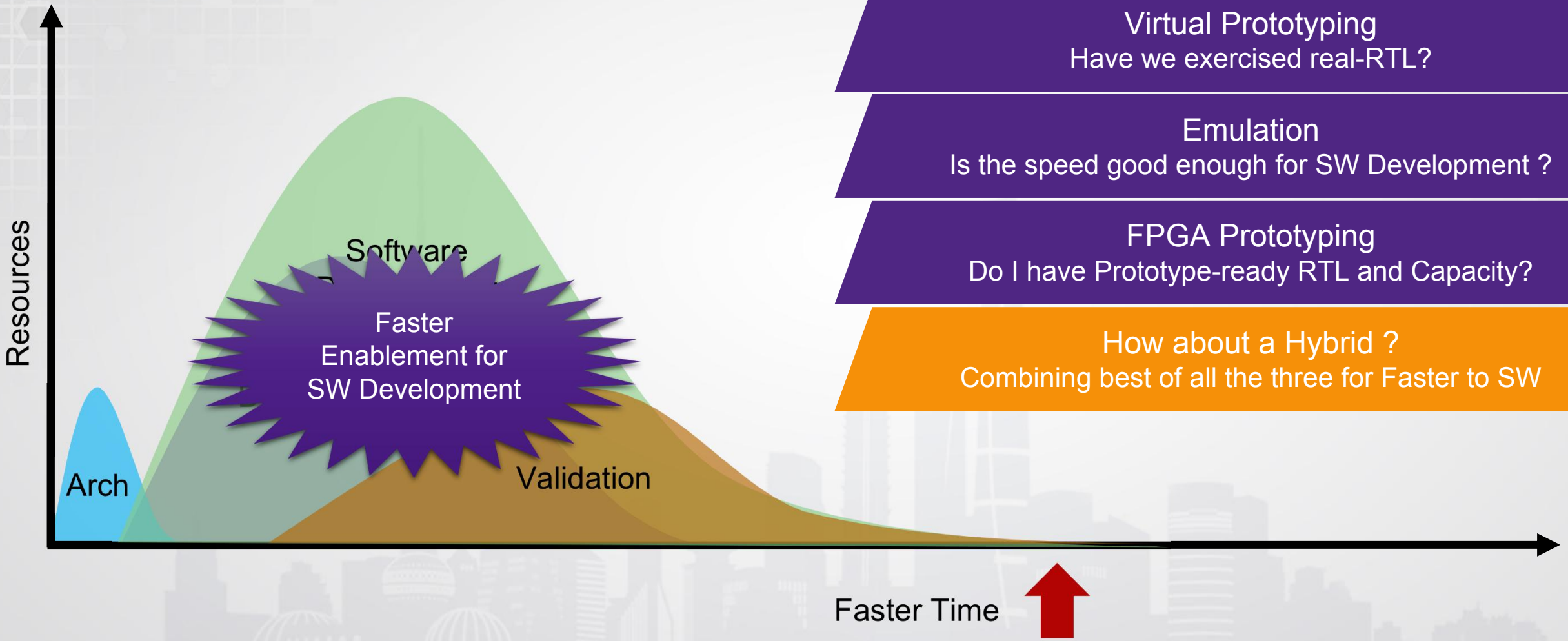

Virtual Prototyping
Have we exercised real-RTL?

Emulation
Is the speed good enough for SW Development ?

FPGA Prototyping
Do I have Prototype-ready RTL and Capacity?

How about a Hybrid ?
Combining best of all the three for Faster to SW

SoC Verification Flow

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Performance & Power – *Architecture Analysis, Optimization & Verification*

Platform Architect	ZeBu	HAPS	Post-Silicon
Architecture Analysis & Optimization	SoC PPA Verification	System Validation	PPA Sign-Off

Software Enablement – *Bring-up, Validation & Optimization*

Virtualizer	Virtual Host	ZeBu	HAPS
Pre-RTL SW Development		HW/SW Verification	Validation & Tuning

Function – *Block & SoC Verification, HW/SW Verification & System Validation*

VC Formal DPV	VCS	ZeBu	HAPS	Post-Silicon
Datapath Verification	Block Verification	SoC Verification	System Validation	Sign-Off

Shift-left with Synopsys Hybrid Solutions

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Performance & Power – *Architecture Analysis, Optimization & Verification*

Platform Architect — Hybrid Performance Analysis — ZeBu — HAPS — Post-Silicon

Shift left

Architecture Analysis & Optimization | SoC PPA Verification | System Validation | PPA Sign-Off

Software Enablement – *Bring-up, Validation & Optimization*

Hybrid Emulation

Virtualizer — Virtual Host — ZeBu — HAPS

Virtual I/O | Hybrid Prototyping

Shift left

Pre-RTL SW Development | HW/SW Verification | Validation & Tuning

Function – *Block & SoC Verification, HW/SW Verification & System Validation*

VC Formal DPV | VCS | ZeBu | HAPS | Post-Silicon

Shift left

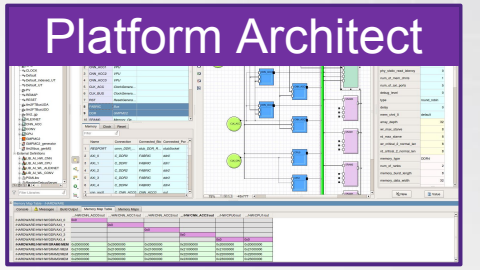
Datapath Verification | Block Verification | SoC Verification | System Validation | Sign-Off

Synopsys Hybrid Solution

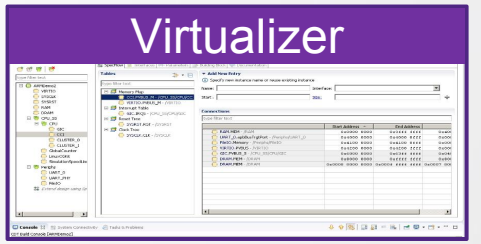
- Hybrid Architecture Analysis
  - Efficient architecture analysis and smart performance monitoring
  - Offline and online analysis of performance data collected on ZeBu
  - Faster PPA optimization, helping shift left verification cycle

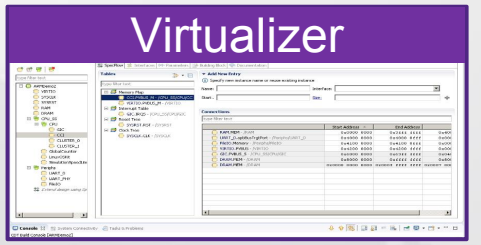
- Hybrid Emulation
  - Early Driver/Firmware/Application development
  - Complete SoC model using VDK and synthesizable RTL IPs
  - Power and performance validation over billions of application cycles

- Hybrid Prototyping
  - Software driven system validation with real-world IO
  - Early Driver/Firmware/Application development
  - Modular and scalable validation from IP to system level



ZeBu





HAPS

Software Driven Verification Project Flow

Production Software Stack → SW Signoff before Tapeout

SoC TLM Model
VDK
10~100+MHz

Hybrid Emulation

CPU Model + IP/SoC RTL
VDK
Hybrid
10+MHz
ZeBu

SoC RTL
ZeBu
1+MHz

SW Driven Full System Validation

SW Development Platform

CPU Model + IP/SubSys RTL
VDK
Hybrid
20+MHz
HAPS

SoC RTL
HAPS
10~200MHz

Hybrid Prototyping

SW Driven IP/Subsystem Validation

Continuous SW Driven Development/Verification Platforms

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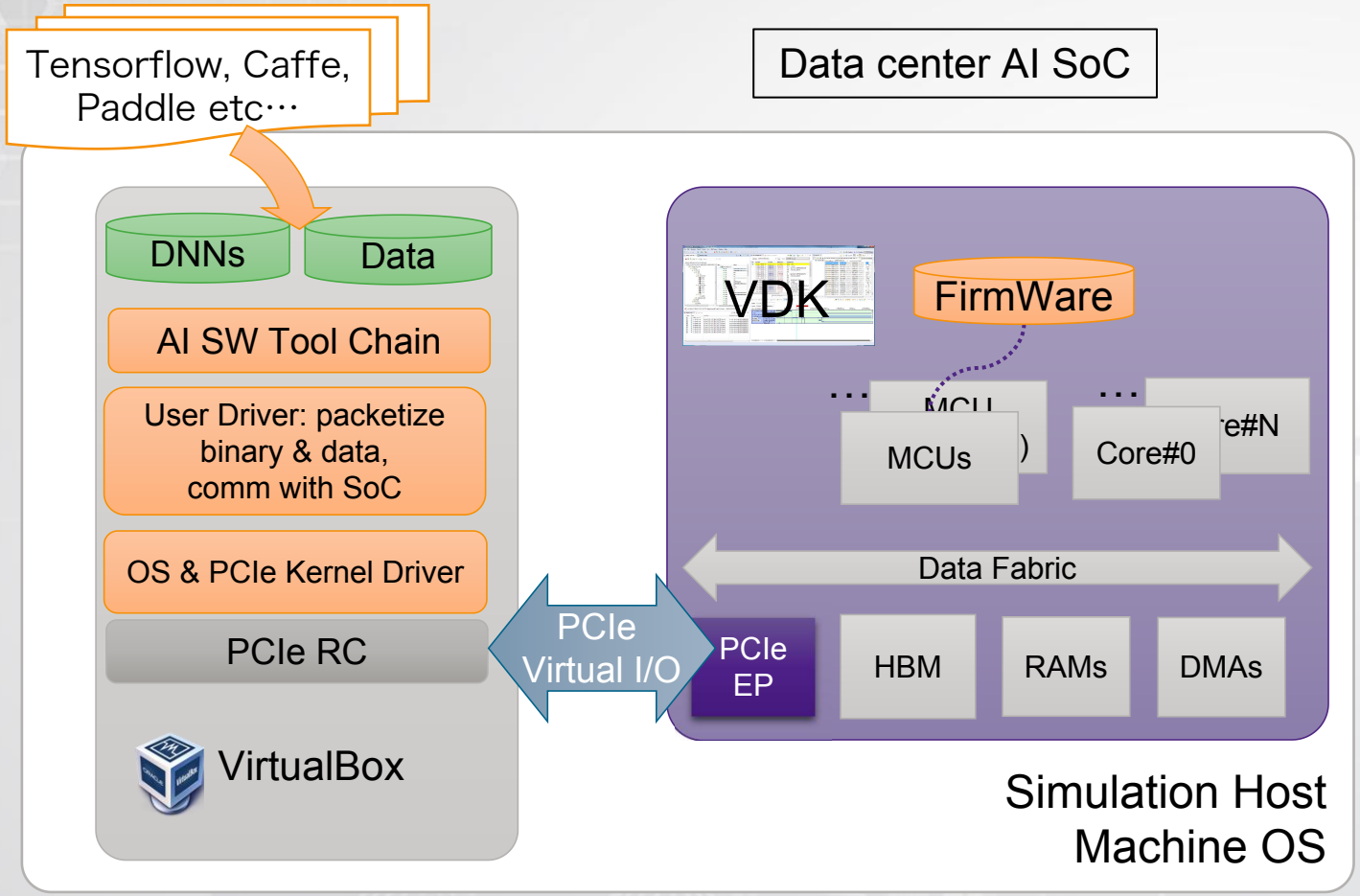
Use Case: Virtual I/O

Using VDK to Bring up AI SoC FirmWare



Design Type : AI SoC

- PCIe Virtual I/O for AI HW/SW Integration & Optimization
- AI Host OS and SW Tool chain SW running on VirtualBox
- VDK connected to VirtualBox via PCIe Virtual I/O

Leading AI SoC Company brings-up SoC FW 3~5 months before RTL

Use Case: Virtual Host

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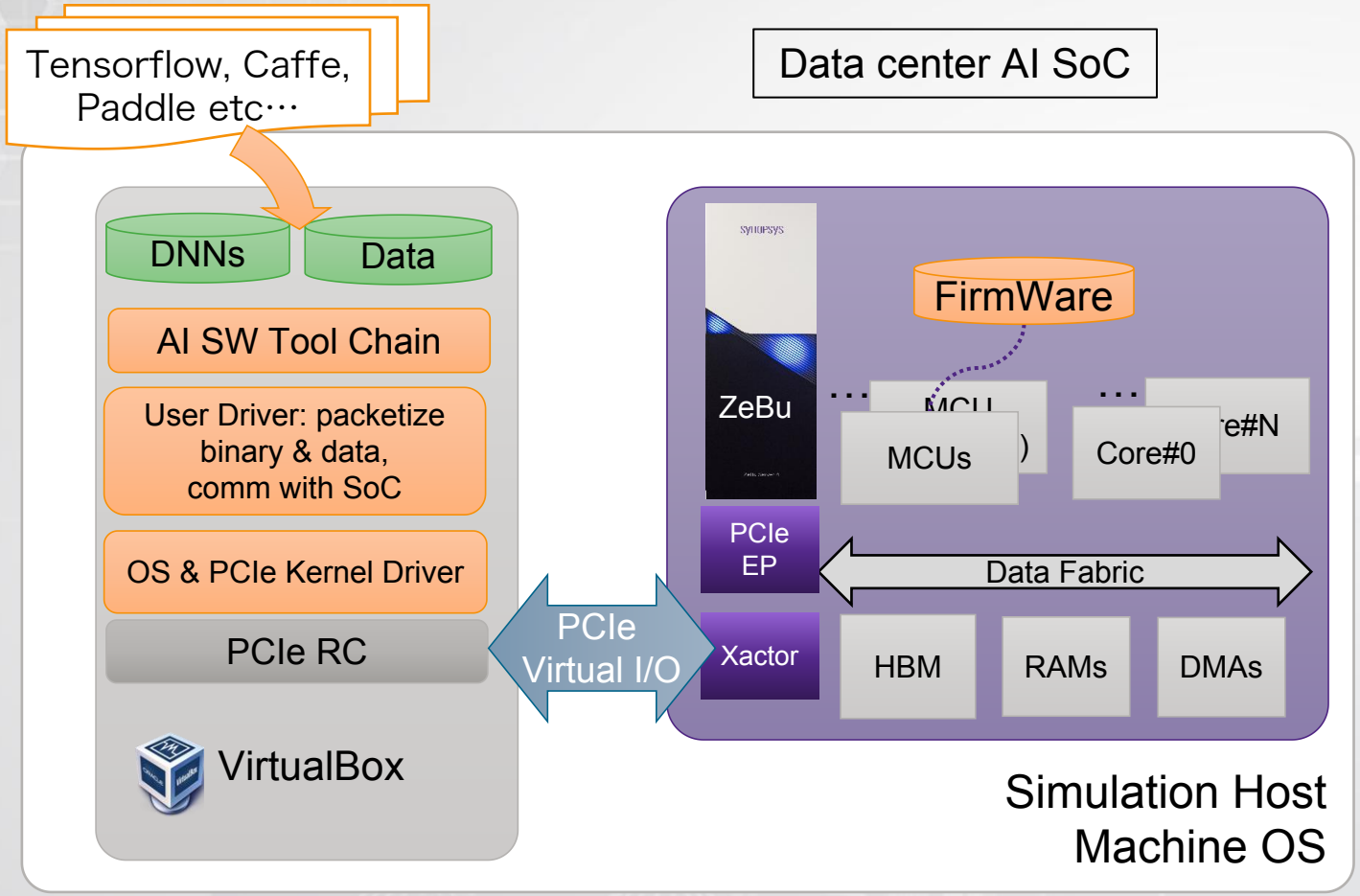
Reuse VirtualBox setup for ZeBu HW/SW validation



Design Type : AI SoC

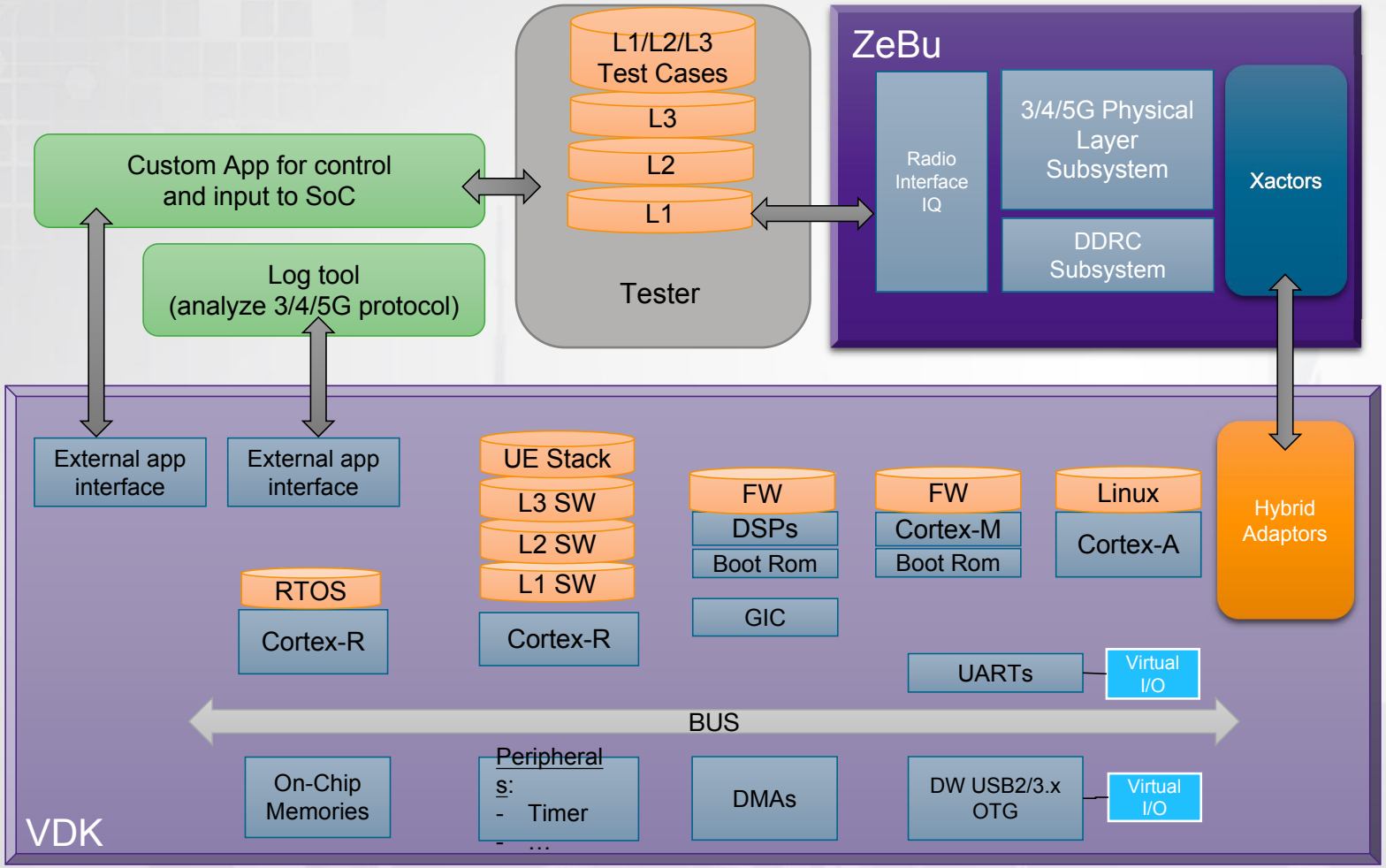
- Same VirtualBox setup
- Speed up HW/SW validation and turning performance
- Re-use mature host side AI SW tool chain, driver, and SoC Firmware develo… based on VDK environment

Detailed article in Chinese published in SNPS WeChat

Smooth Transition to Emulation for Validation

Use Case: Hybrid Emulation

5G Modem Full HW/SW Verification Platform



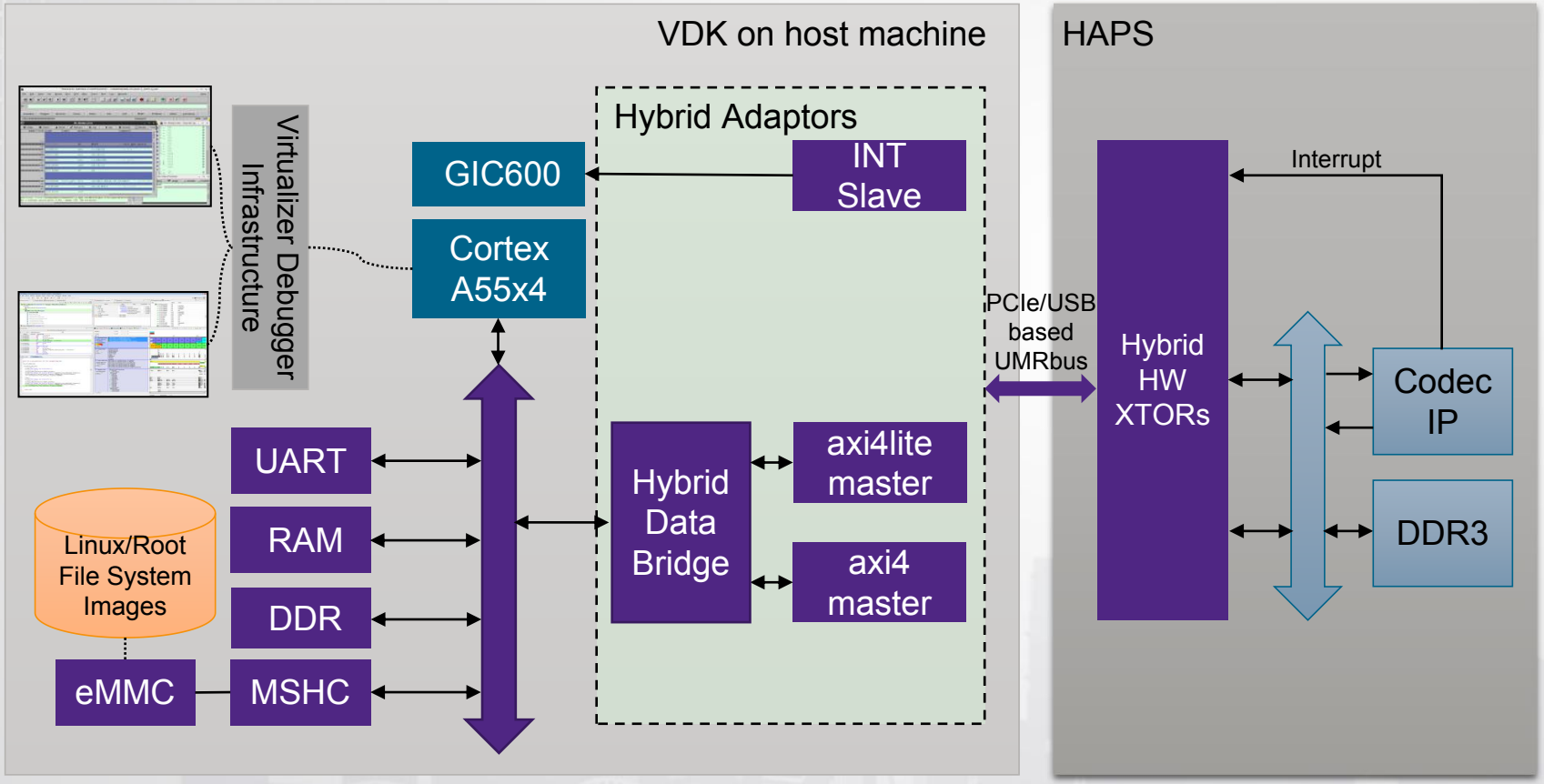
Design Type : 5G Modem

- Start full-stack 5G HW-SW co-verification and testing 6~9 months earlier
- OS boot within 10 minutes - run one 5G case in 15 min
- Users identified more than 100 HW/SW issues on hybrid platform before tape out
- More productive HW/SW

Leading Networking Company Starts Full-stack 5G Co-verification 6-9 months earlier

Use Case: Hybrid Prototyping

Accelerating SW Development and RTL Validation



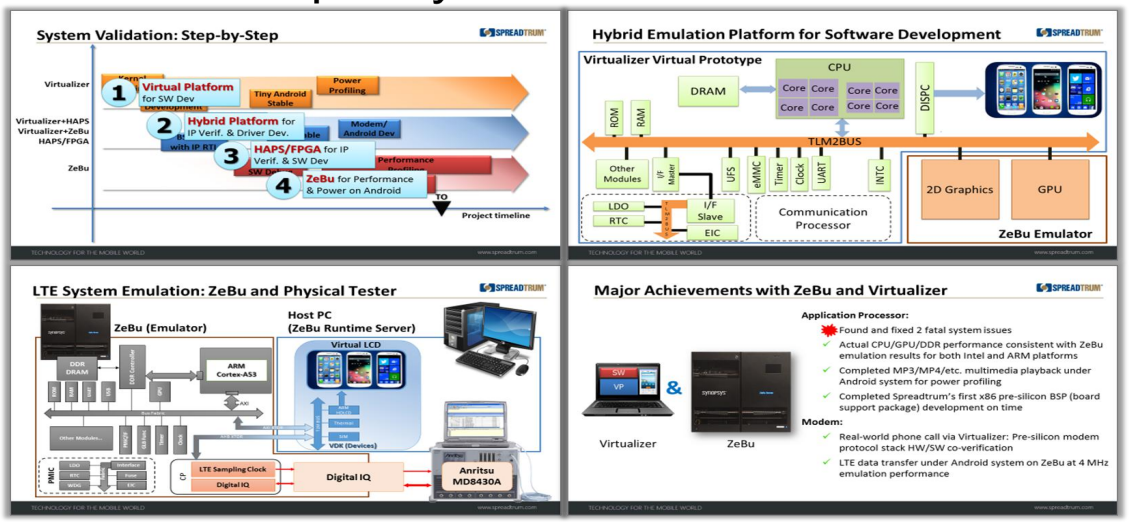
Design Type : Drone SoC

- Easy Setup
  - VDK with custom OS
  - Different IPs in HAPS
  - Smaller prototype
  - Faster prototype compile
- Debug Productivity
  - Boots OS in <1 minute
  - OS trace/profiling helps HW/SW debug and SW performance analysis
  - Full HW debug visibility for registers/pins
- Fast Speed
  - 4K 100 Frames Encoding took 3mins to complete in hybrid, while in pure FPGA it

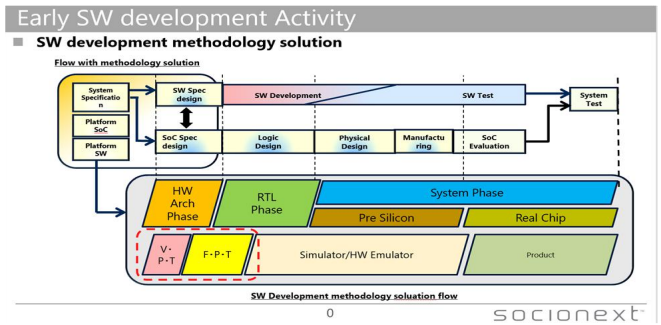
Leading Asia Drone Company boots Linux in <1 minute

Customer Successes

Spreadtrum Adopts Hybrid for AP & Modem SoC



Socionext Hybrid Prototyping



FPGA Prototyping
- Difficult to implement large SoC to 1 chip FPGA
- Implement too huge circuit effect to performance
- Divide to multiple FPGA has more load

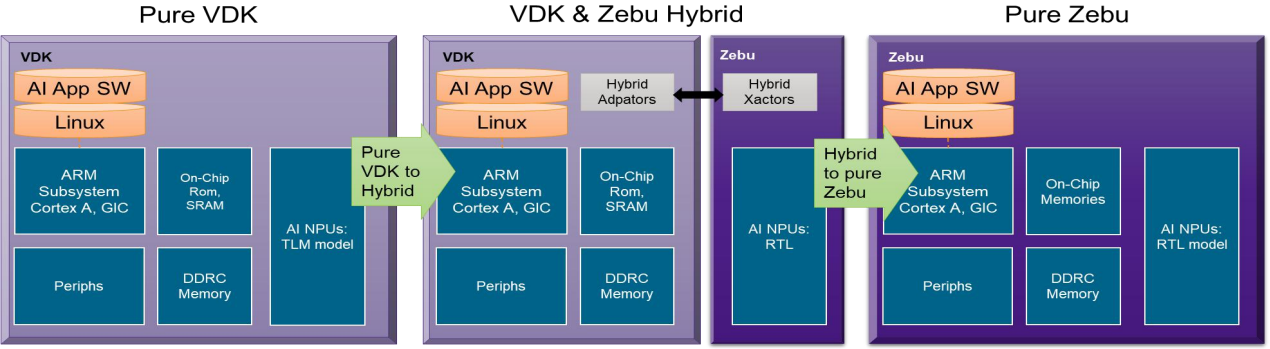
Smooth connection to SW design env

Hybrid Prototyping
- Minimize circuit implementing to FPGA
- Reduce risk to slow performance
- Use VDK for CPU sub system
- Flexible to connect SW design flow
- Easy to chance memory map
- Reuse by changing target IPs

Create VPF of common platform
- Good usability
- Early start of OS porting/basic SW development

Use as internal tool
Use as sales tool for external customer

Successful AI Edge Design Case: A Leading AI System Company
VDK → Hybrid→ Zebu Smooth Design/Verification Flow



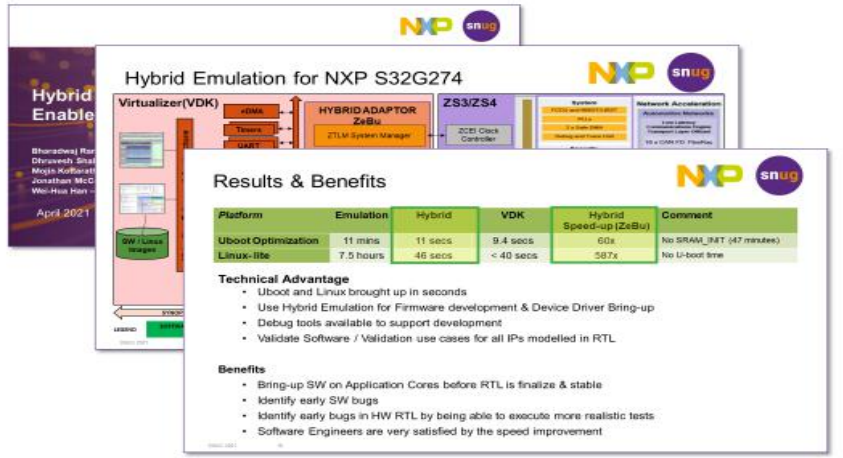
- Start SW dev 3~6 month earlier with VDK
- Linux boots successfully in 30s in VDK
- Explore SW architecture flow in VDK
- Develop SW testcases for HW verification
- AI SW compiler tool chain testing and validation based on VDK
- SW img. load at runtime after Linux boot

- Same SW run in VDK and Hybrid
- IP & Subsystem validation testcases run in minutes in hybrid; in pure EMU run hours to boot Linux and do testcase on top of it
- SW img. load at runtime after Linux boot
- Save design size in Zebu as rest of design in VDK side

- Same SW run in VDK, Hybrid and Zebu
- Using pure emulation to do HW/SW final validation
- Less SW debug in pure emulation as SW tested/debugged in VDK or hybrid platforms

Hybrid Emulation for faster SW development

Presented by NXP and Synopsys at SNUG World 2021



- Increasing demand for software bring-up on emulator for complex embedded multicore SoCs
- Hybrid emulation technology provides shift-left approach and helps to reduce risk and cost
- Fast setup with large library of models and transactors in Virtualizer and ZeBu
- Hybrid FastMem technology enables high simulation speed for shared memory access
- Planning to setup automated regression tests and explore power and performance use-cases

Customer Successes

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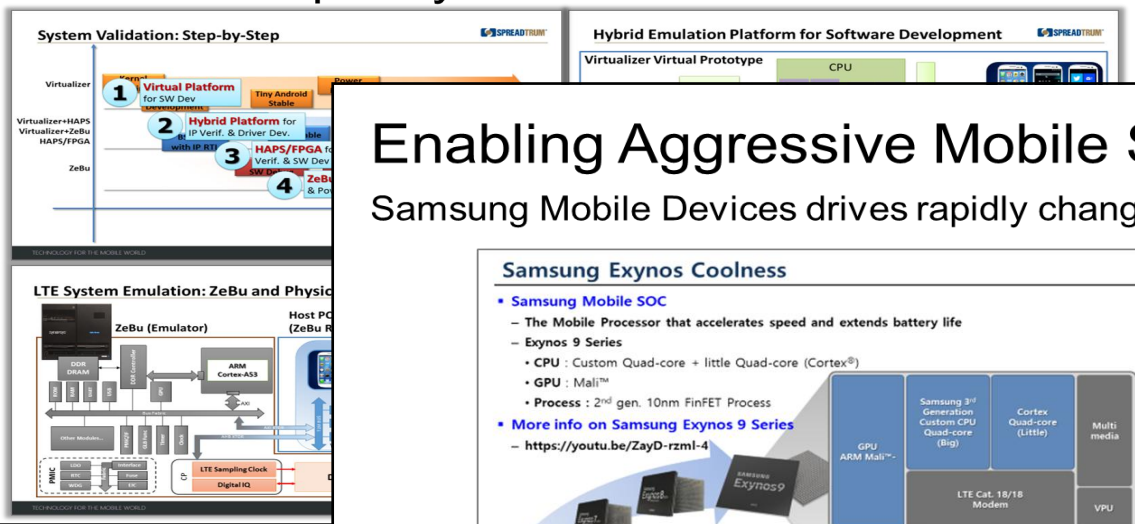

Socionext Hybrid Prototyping

Early SW development Activity

FPGA Prototyping
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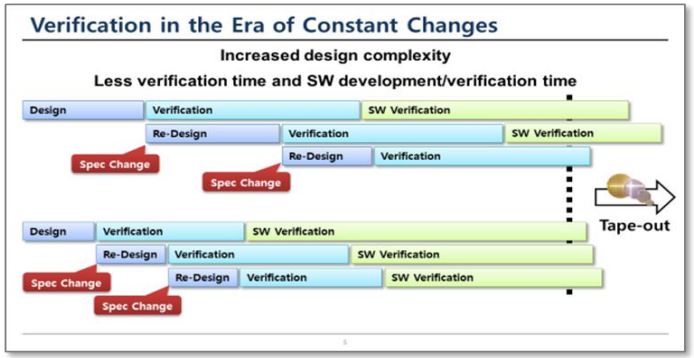
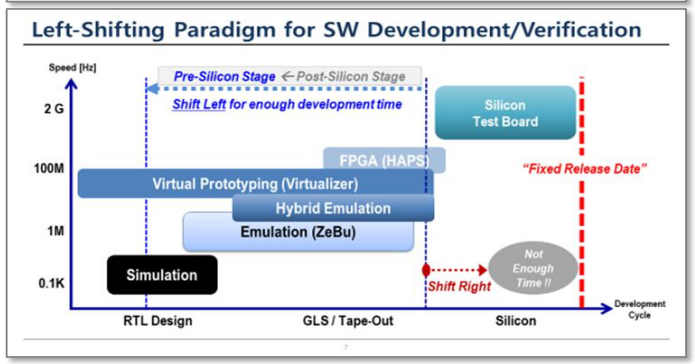
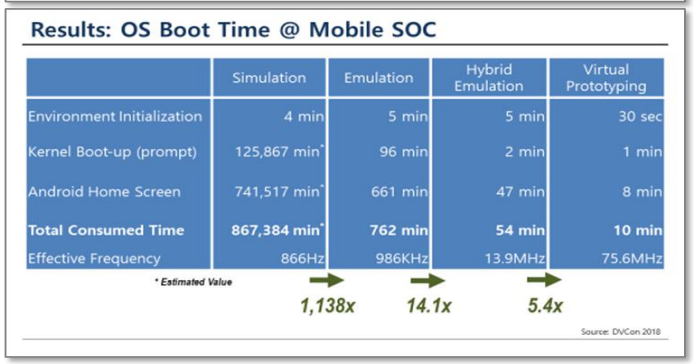
internal tool
sales tool for external customer

Enabling Aggressive Mobile SoC Schedules

Samsung Mobile Devices drives rapidly changing requirements: Samsung SLSI delivers on time







	Simulation	Emulation	Hybrid Emulation	Virtual Prototyping
Environment Initialization	4 min	5 min	5 min	30 sec
Kernel Boot-up (prompt)	125,867 min*	96 min	2 min	1 min
Android Home Screen	741,517 min*	661 min	47 min	8 min
Total Consumed Time	**867,384 min***	**762 min**	**54 min**	**10 min**
Effective Frequency	866Hz	986KHz	13.9MHz	75.6MHz

* Estimated Value

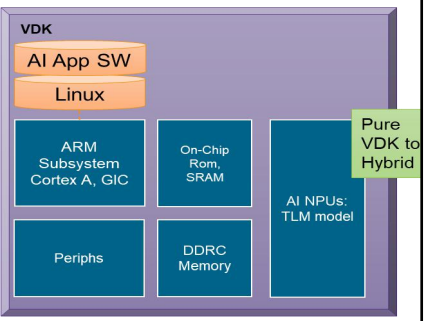
1,138x 14.1x 5.4x

Source: DVCon 2018

DAC 2018

Successful AI Edge D… VDK → Hybrid → Zebu

Pure VDK



Pure VDK to Hybrid

- Start SW dev 3~6 month earlier with VDK
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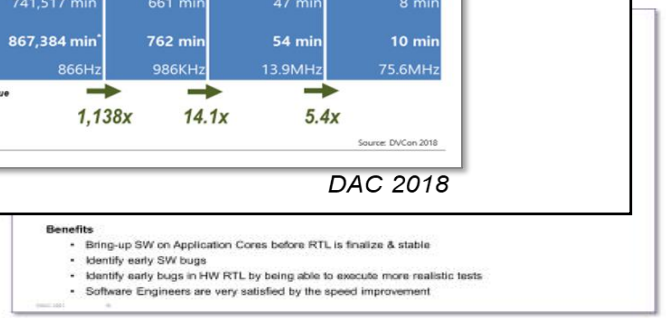

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NXP

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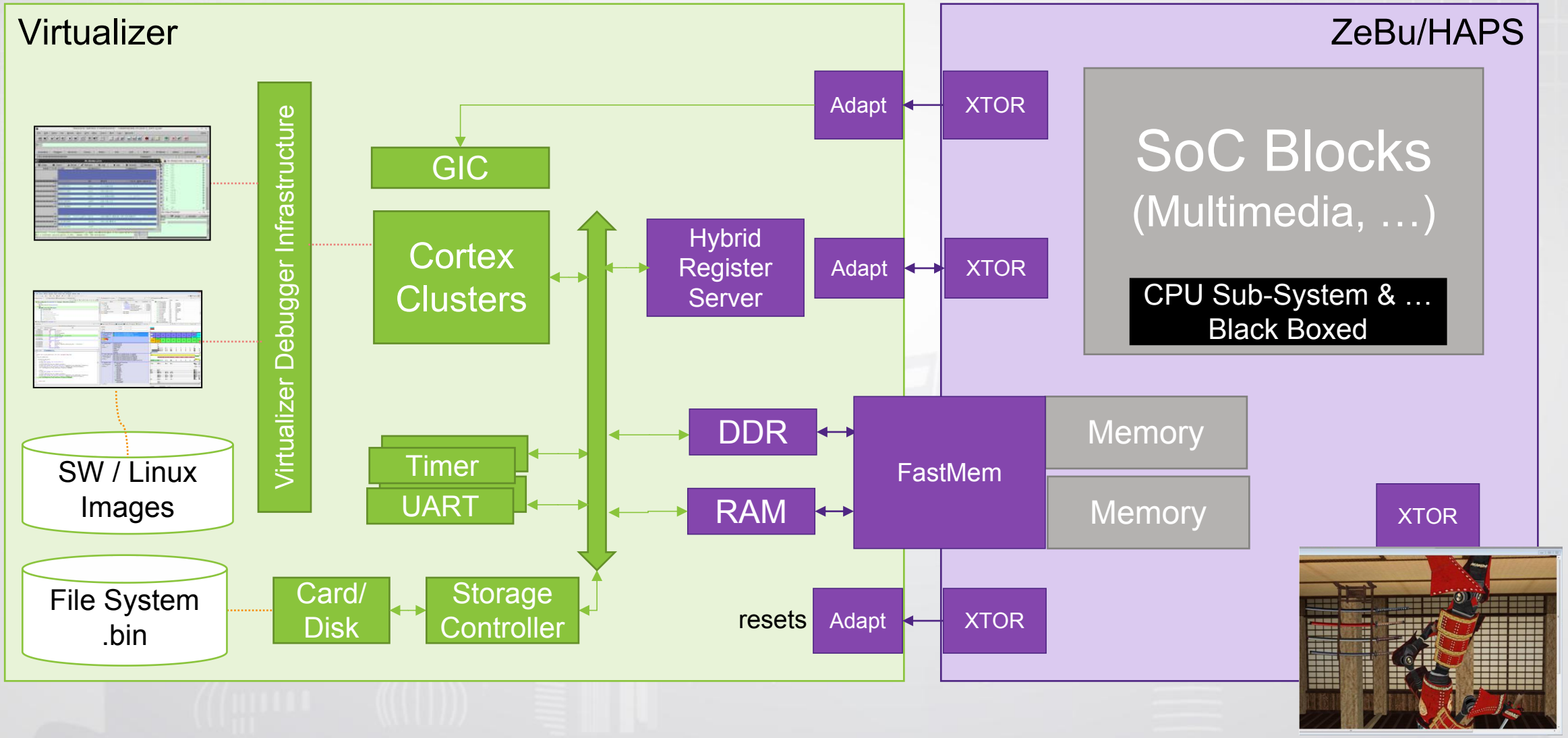
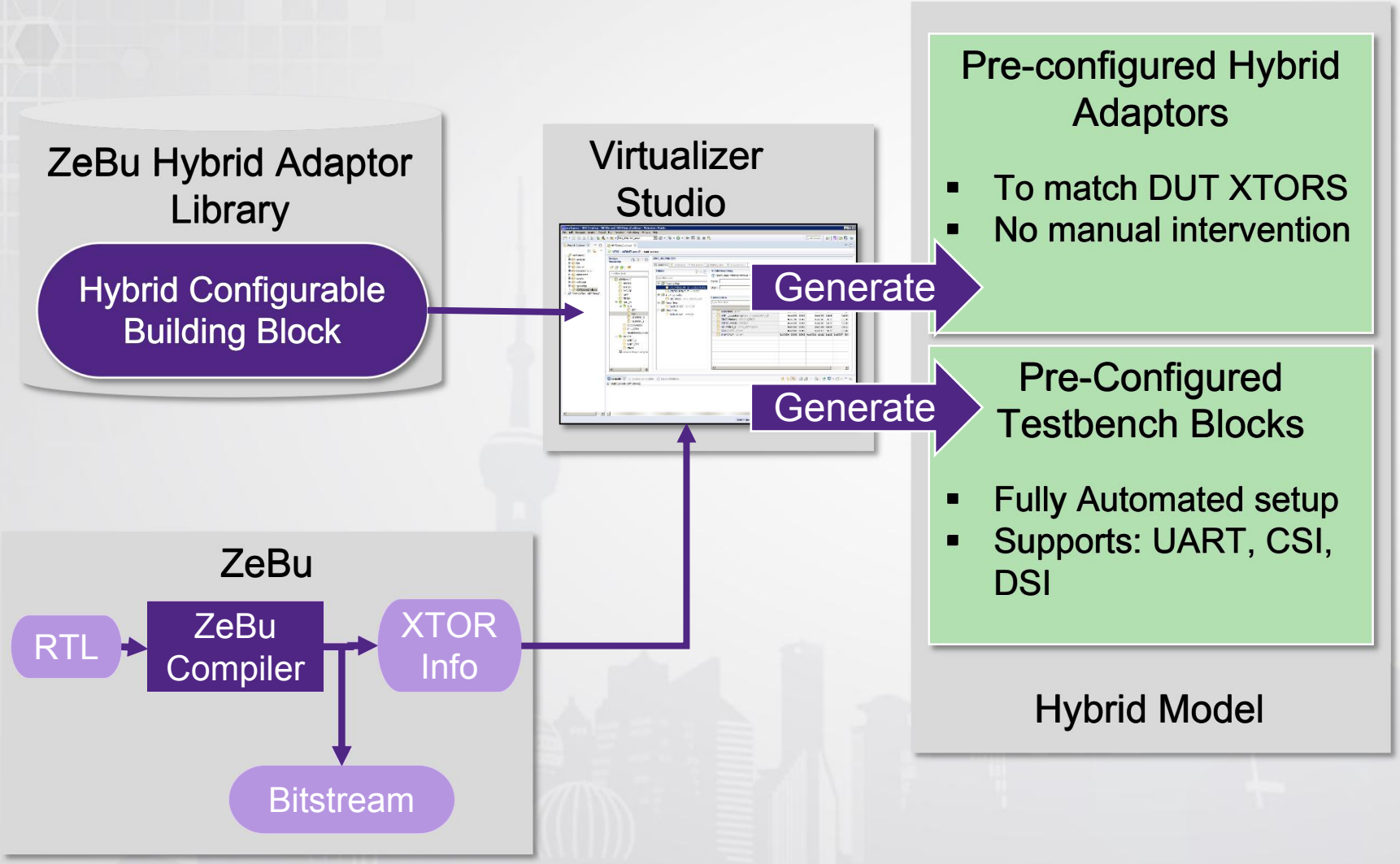
Typical Hybrid Block Diagram Overview



10x Faster Hybrid Creation

Configurable Hybrid Building Block



- 10x faster Hybrid setup
- Fully Automated
- Correct by construction
- Pre-configured ZeBu Testbenches for UART/CSI/DSI
- Automatically generate templates for Custom monitors and testbenches

Higher Hybrid Debug Productivity

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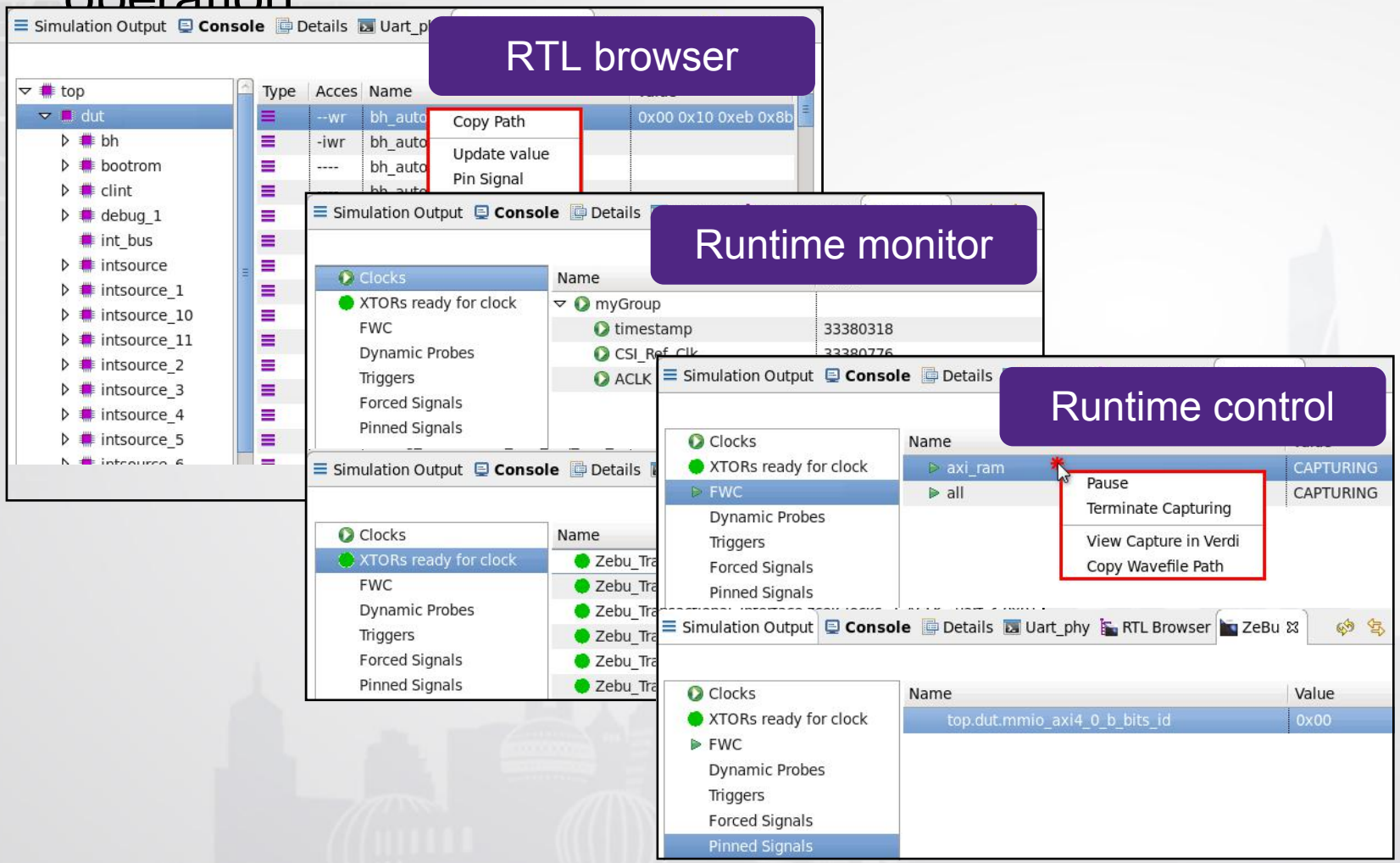
Unified ZeBu-Virtualizer views for Single-window operation



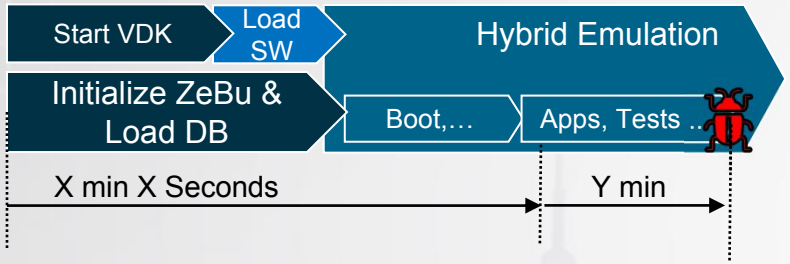
- RTL browser
  - ✓ Access to all DUT signals
- Runtime monitor
  - ✓ System Clock Status
  - ✓ XTORs Readiness Status
- Runtime control
  - ✓ Waveform dump (FWC, QiWC, Dynamic Probe)
  - ✓ Triggers
  - ✓ Forces

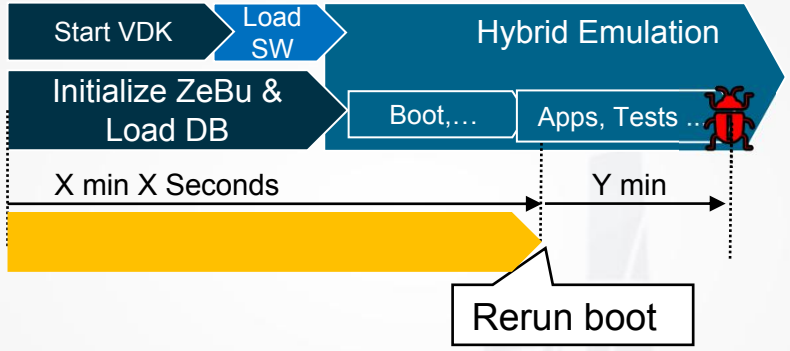
Hybrid Checkpoint Restore

Enables fast turn around time for boot & run, debugging

Standard Sequence

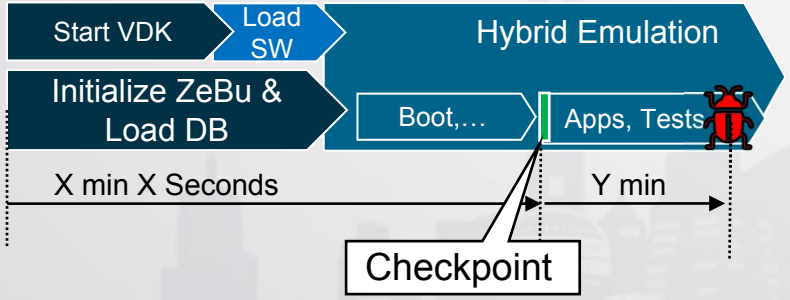
Run through the OS Boot, load & run applications

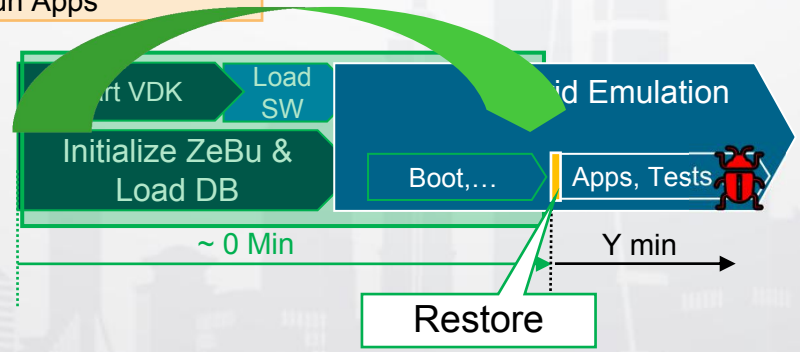




Checkpoint-Restore Sequence

Boot OS, Checkpoint, Run Apps etc
Next time: Restore, Run Apps

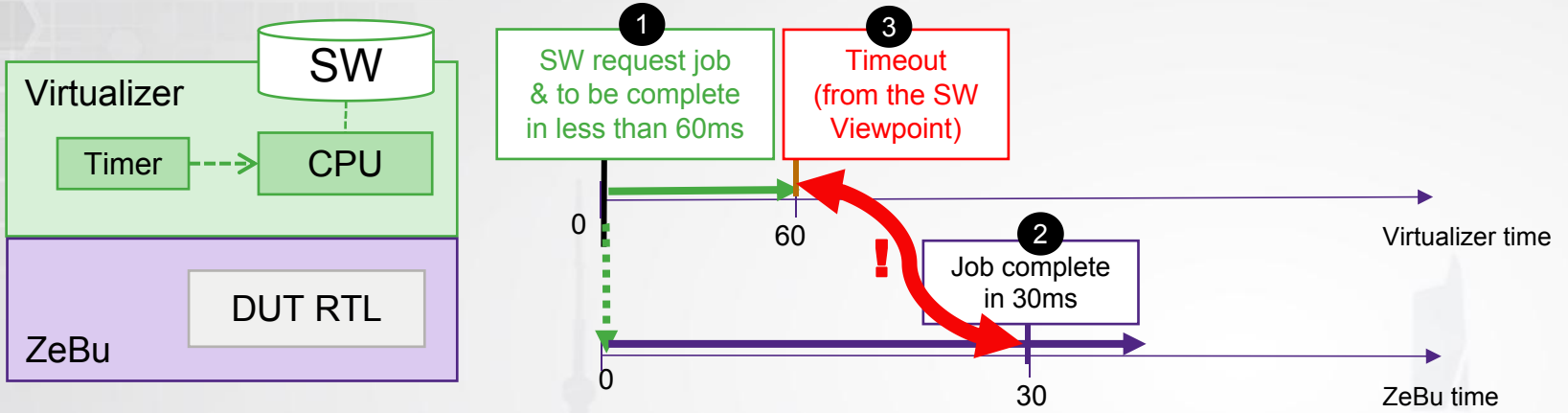


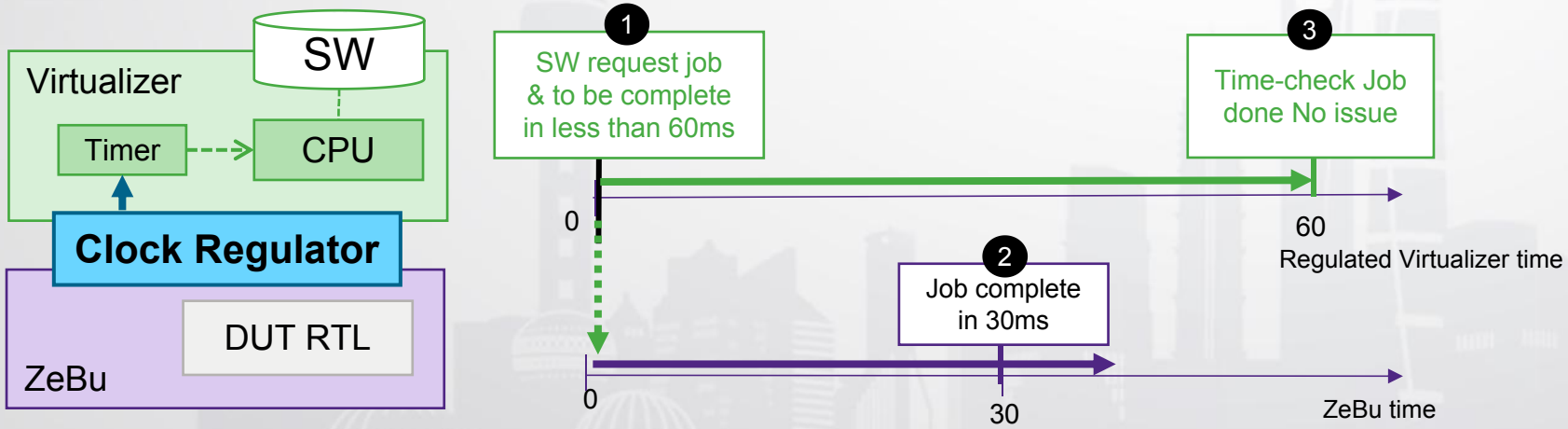


- Bypass boot sequence for consecutive tests
- Save Hybrid Setup
  - HW DUT in ZeBu
  - Virtualizer Platform including files and configurations
- Restore Hybrid State

Hybrid Clock Regulator

Time alignment between Software and Hardware



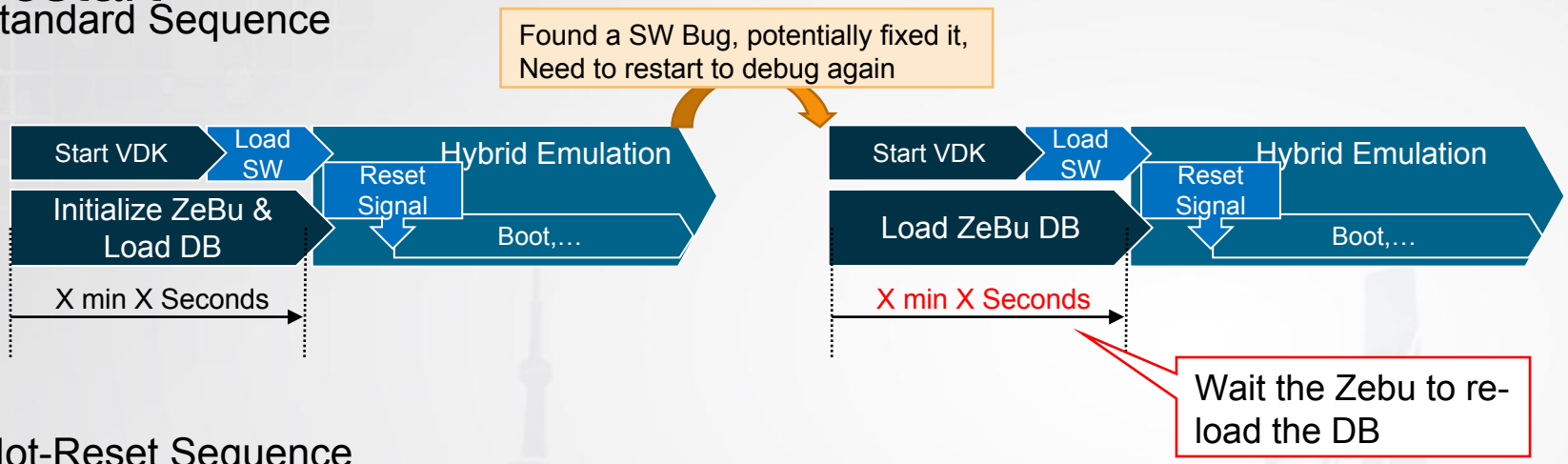


- Purpose
  - Resolve timeout issues between Fast (Software) and Slow (DUT in Hardware) side Hybrid components
  - Maintain speed
- Technology
  - Clock regulator to align timer in Virtualizer with execution in ZeBu
  - No need to “hack” Software
  - No trial and error to figure out timer & ZeBu clock settings

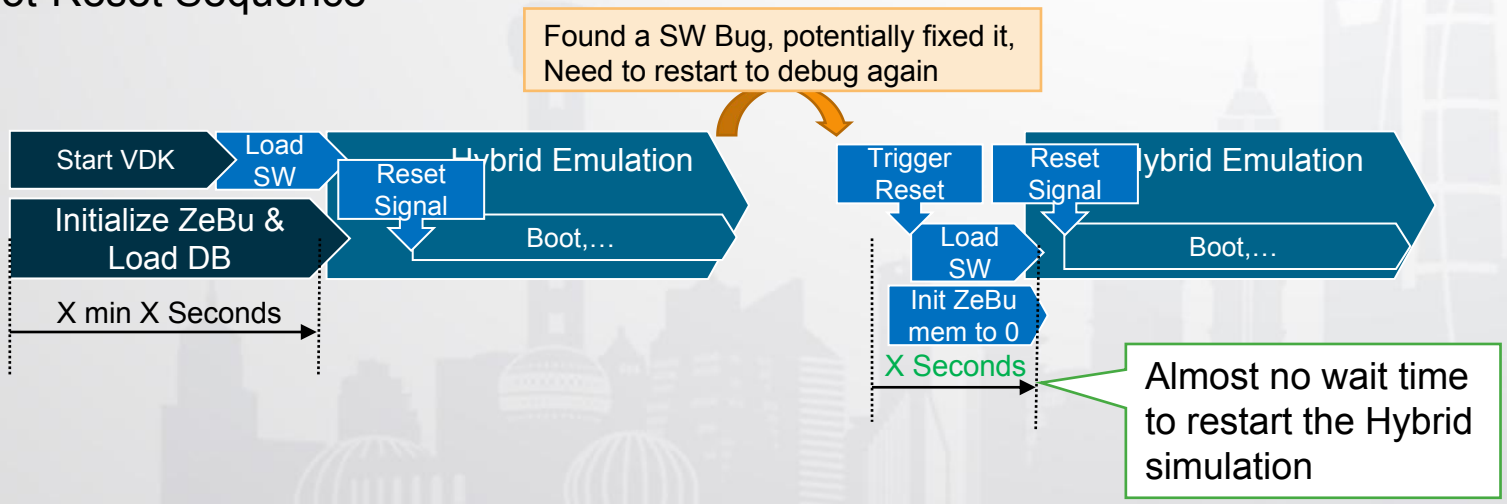
Faster Debug with Hot Reset

Accelerate the debug TAT by faster Hybrid emulation restart

Standard Sequence



Hot-Reset Sequence



- Reduce the restart time to only a few seconds
- No Design Database reload
- Load and test multiple SW Images at Runtime

Validate Performance at High Speed

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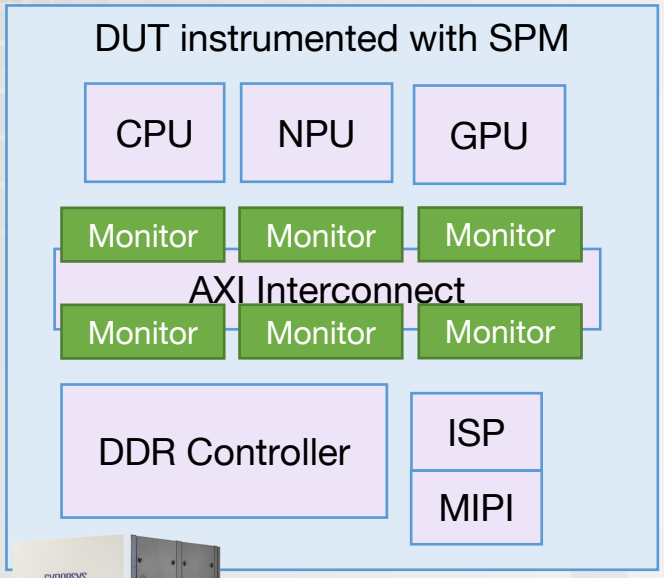
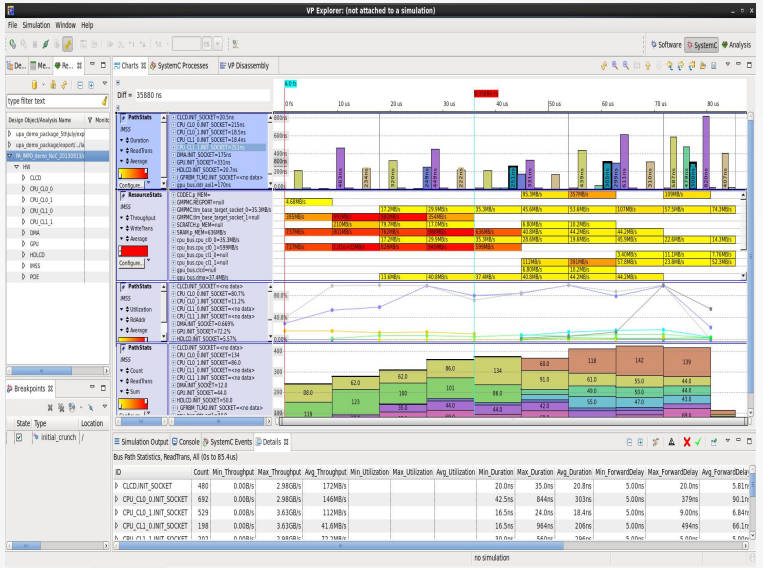
Smart Monitors for Performance and Transactional Analysis

ZeBu



- SV insertion in DUT
- Fast pre-processing
- Fast DPI-C interface

Platform Architect



- Automatic launch & configuration
- Fast & efficient analysis database
- Stream performance analysis
  - Batch / Post-run
  - Dynamic / On-line

- Performance monitoring at SoC Interconnects
  - Throughput, Latencies Command/Data/ Transactions
  - Assertion-based max command latency violation checks
- Transactional Monitoring for Memories and Bus Interfaces
- < 5% emulation speed impact

Conclusion

- Software and System Validation drives more than 50% of design cost and timelines
- Early HW/SW system verification is key for time to market
- Synopsys Hybrid is widely adopted in the industry to address early HW/SW system verification
- Synopsys has the largest investment in virtual prototyping, emulation and continues to innovate in new hybrid technologies

Thank You

Q & A