2021 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA
SHANGHAI | MAY 26, 2021

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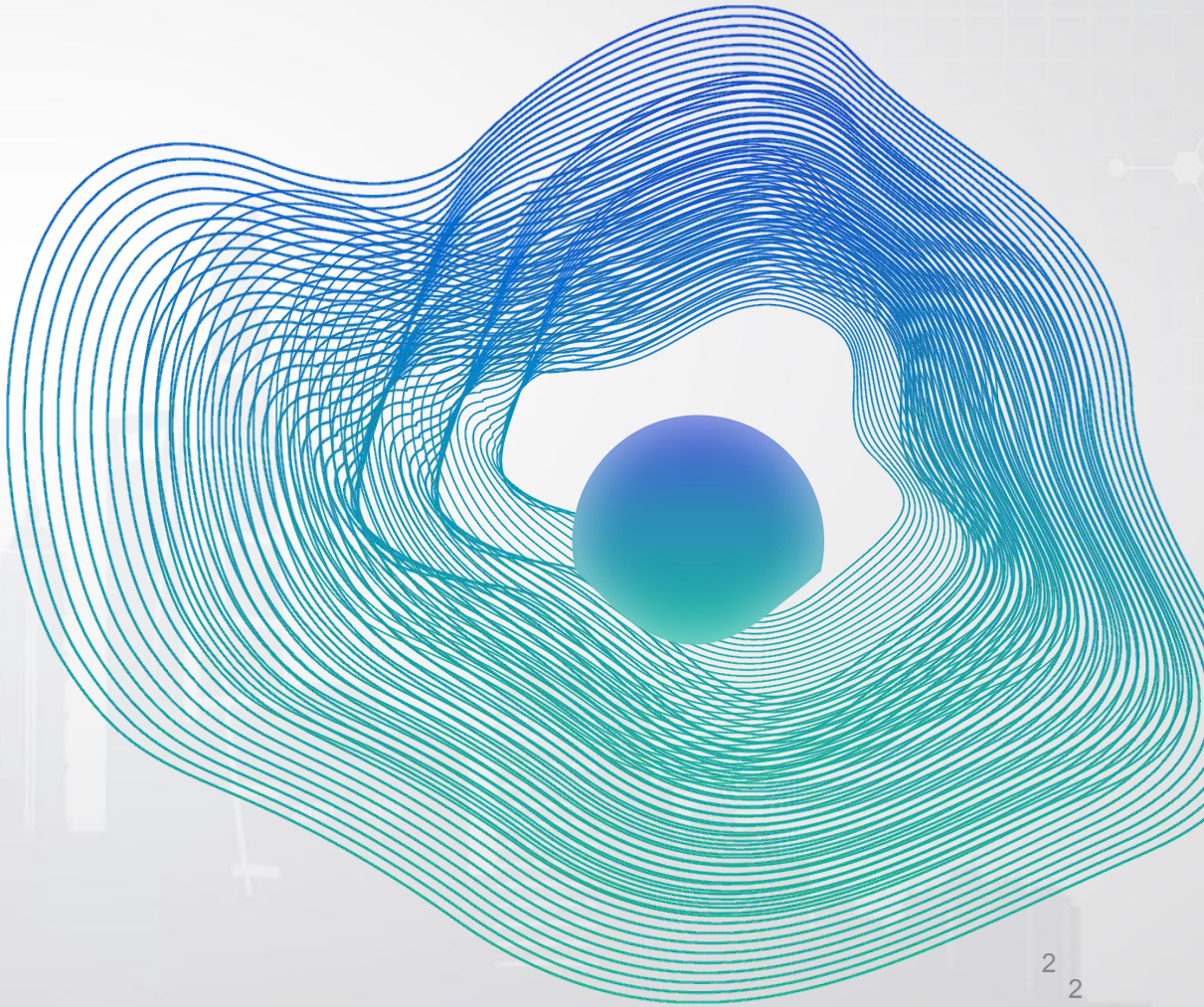
芯华章

应用PSS进行智能化验证

David Hwang and Sera Gao from X-Epic

芯华章公司介绍

芯华章聚集全球EDA行业精英和尖端科技领域人才，致力于面向未来的新一代EDA软件和智能化电子设计平台的研发，产品将全面覆盖数字芯片验证需求，包括：硬件仿真系统、FPGA原型验证系统、智能验证、形式验证以及逻辑仿真，全面助力集成电路、5G、人工智能、云服务、汽车电子和超级计算等多领域的发展，为合作伙伴提供自主研发、安全可靠的芯片产业解决方案与专家级顾问服务。



芯华章验证产品将覆盖

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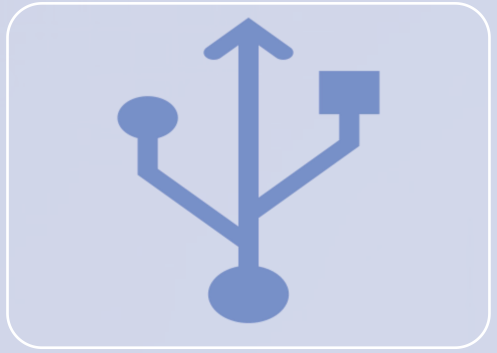
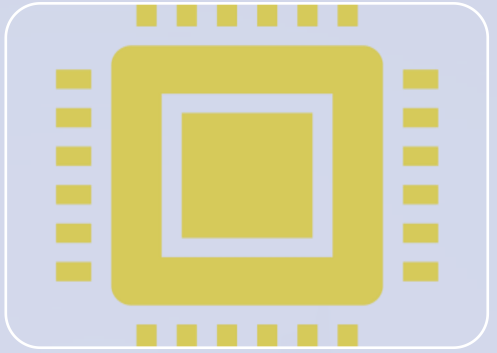
硬件仿真系统	FPGA原型验证	形式验证	智能验证	逻辑仿真
Hardware Emulation System	FPGA-based Prototyping	Formal Verification	Intelligent Verification	Logic Simulation

跨平台激励应用在芯片验证不同阶段






IP level

利用atomic seq构造各种IP级别测试场景

SubSystem

复用IP级的测试用例，快速构建相对复杂的测试场景

SoC level

场景的有效随机率和覆盖率比传统验证方式大大提升

Post-Silicon

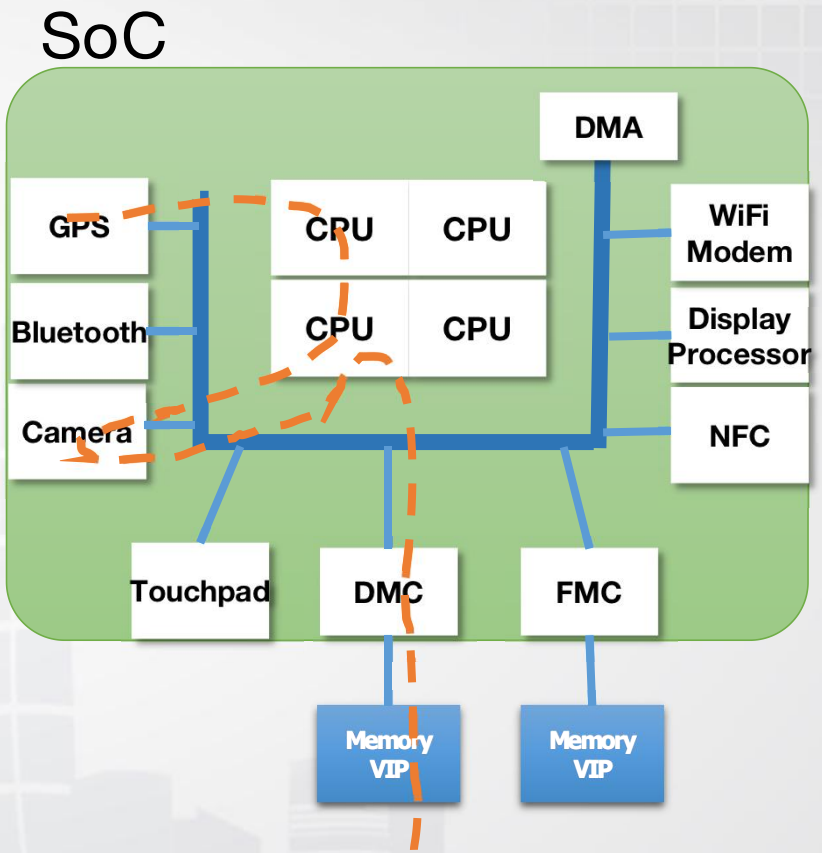
在系统芯片上测试真实的随机场景，分析芯片的性能和功耗

验证遇到的严峻的挑战

验证所有的访存路径

1. GPS – CPU – CAM – DMA -- DMC
2. PAD – CPU – WIFI – DMA – DMC
3. NFC – FMC – CPU – PAD – DMA – DMC
4. ……

```
component soc_top {
  dma_c dma;
  ip_c ip_util;
  pool dbuf dbuf_p;
  bind dbuf_p *;
  action dramtest_a {
    activity {
      do dma_c::dram_xfer;
    }
  }
}
```



跨平台激励技术关键点


提取设计的意图


粗略描述场景

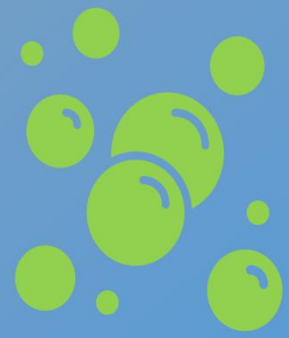

场景组合


形式语言表达
formal description

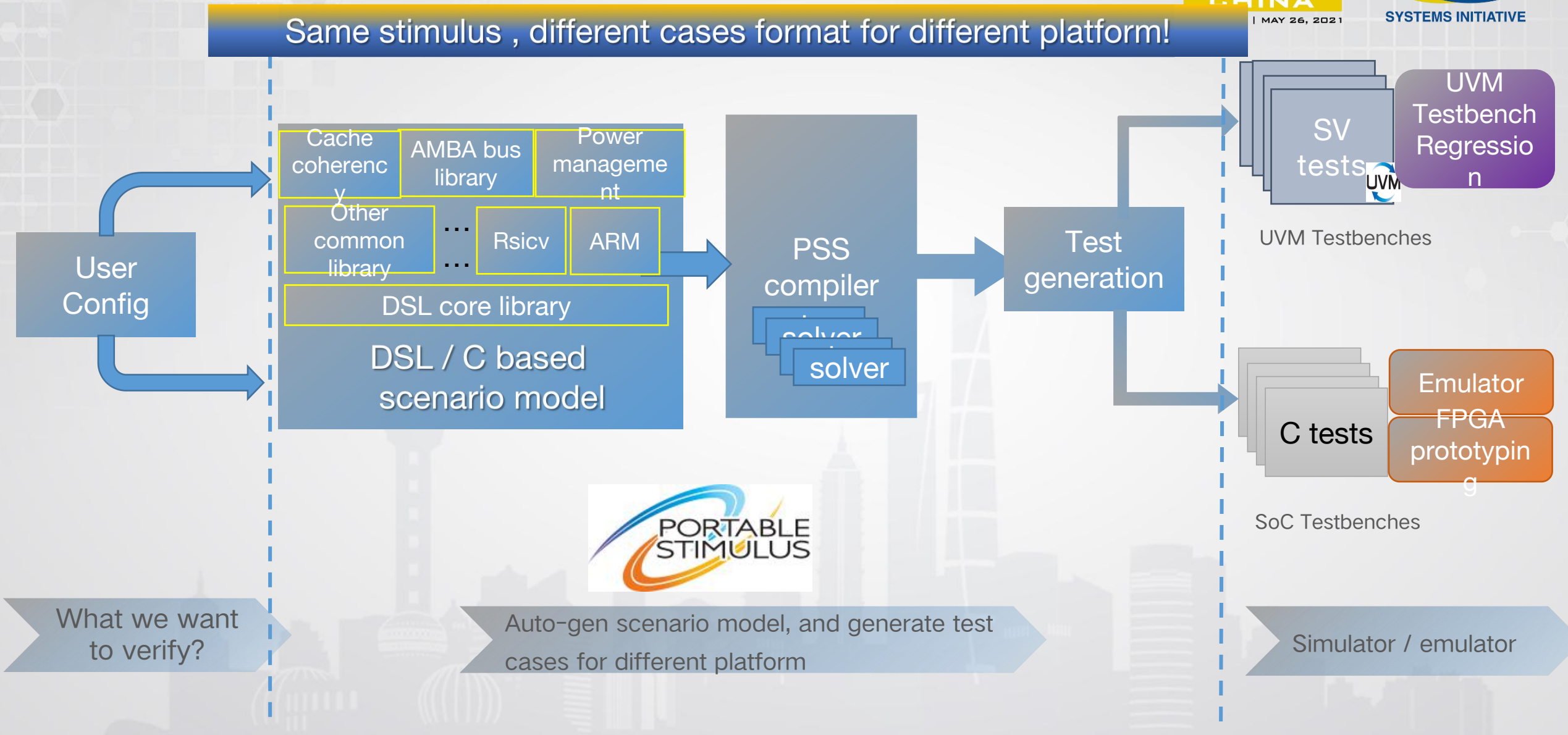

场景自动生成


多目标平台运行

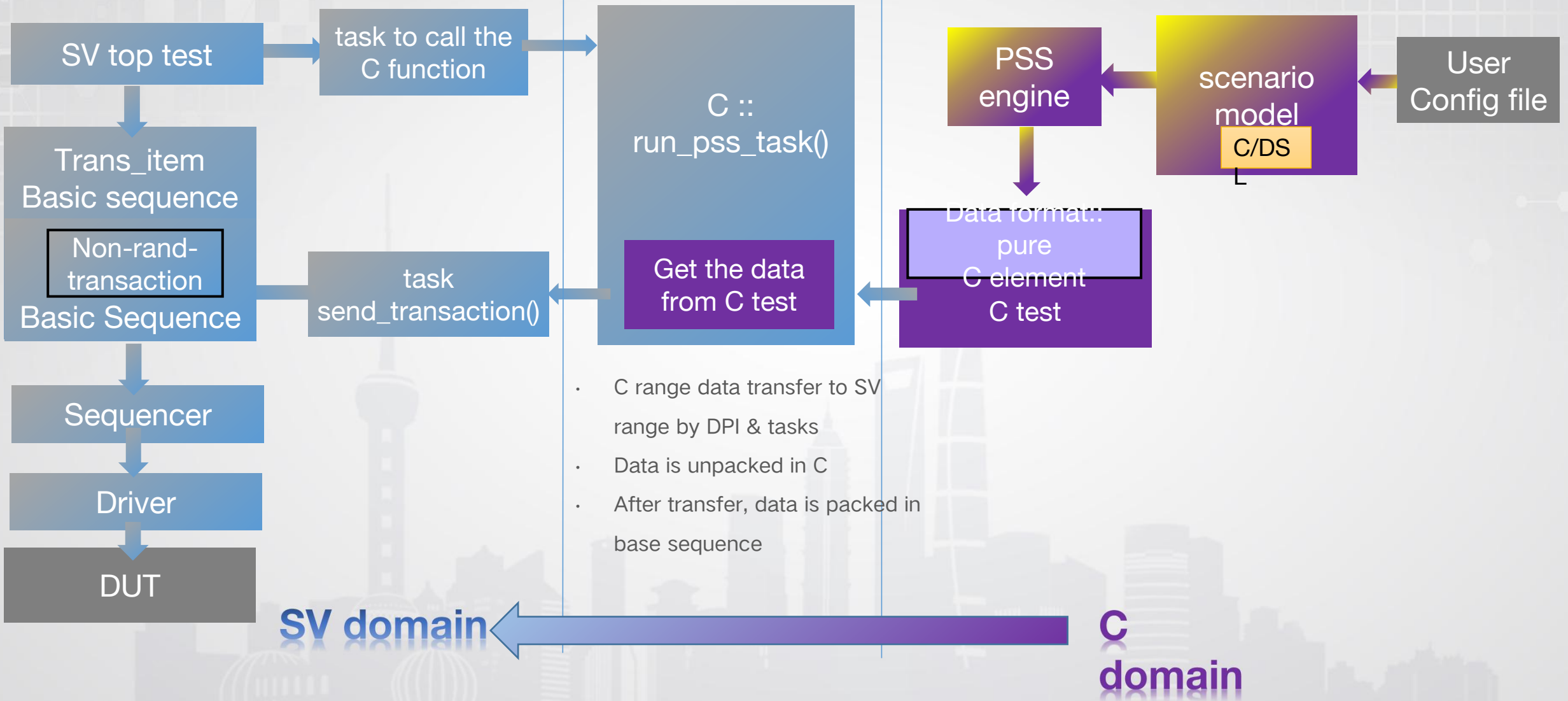
- PSS对测试场景具有高效建模和表达方式
- 能够快速有效地提高系统级测试覆盖率
- 用单一语言产生多目标平台的测试场景



跨平台激励工具的使用流程



SV case的生成实例



- C range data transfer to SV range by DPI & tasks
- Data is unpacked in C
- After transfer, data is packed in base sequence

C和SV测试用例中的数据结构


```
bit [31:0] addr[16],
bit [31:0] data[16],
bit        rd_or_wr,
int        burst_type,
int        hsize,
int        length
```

DPI & tasks

```
struct burst_packet {
  rand bit in [0..65535] start_addr;
  rand operation_type oper_t;
  rand burst_type burst_t;
  rand transfer_size transfer_s;
  rand bit in [0..65535] length;
```

Transaction in UVM TB

ahb_master_transaction

Transaction in PSS

```
action 4_master_ahb {
    master m1, m2, m3, m4;
    constraint {
        (m1.mID==1);
         m1.read_weight ==100%;
         m2.write_weight == 50%;
         ……
    }
}
```

```
action master {
……
Activity {
    select{ [$read_weight]:  do read.with( constrain);}
    }
}

action write {……}
action read  {……}
```

One action as one time of write /read operation, Very flexible combination between actions, cross layer, cross type

DSL语言 – 高级场景建模

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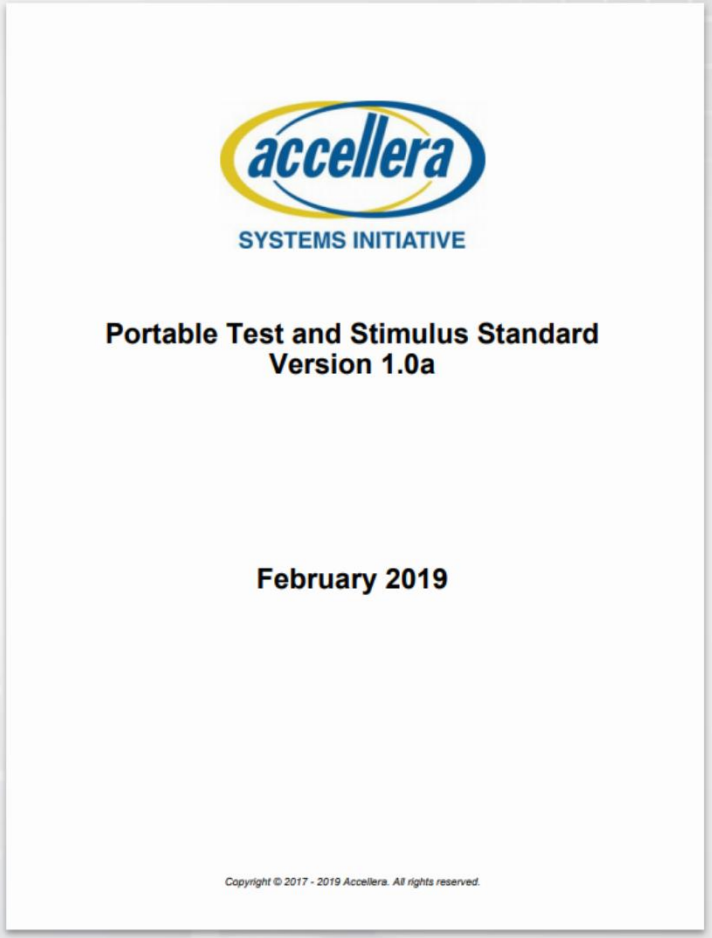
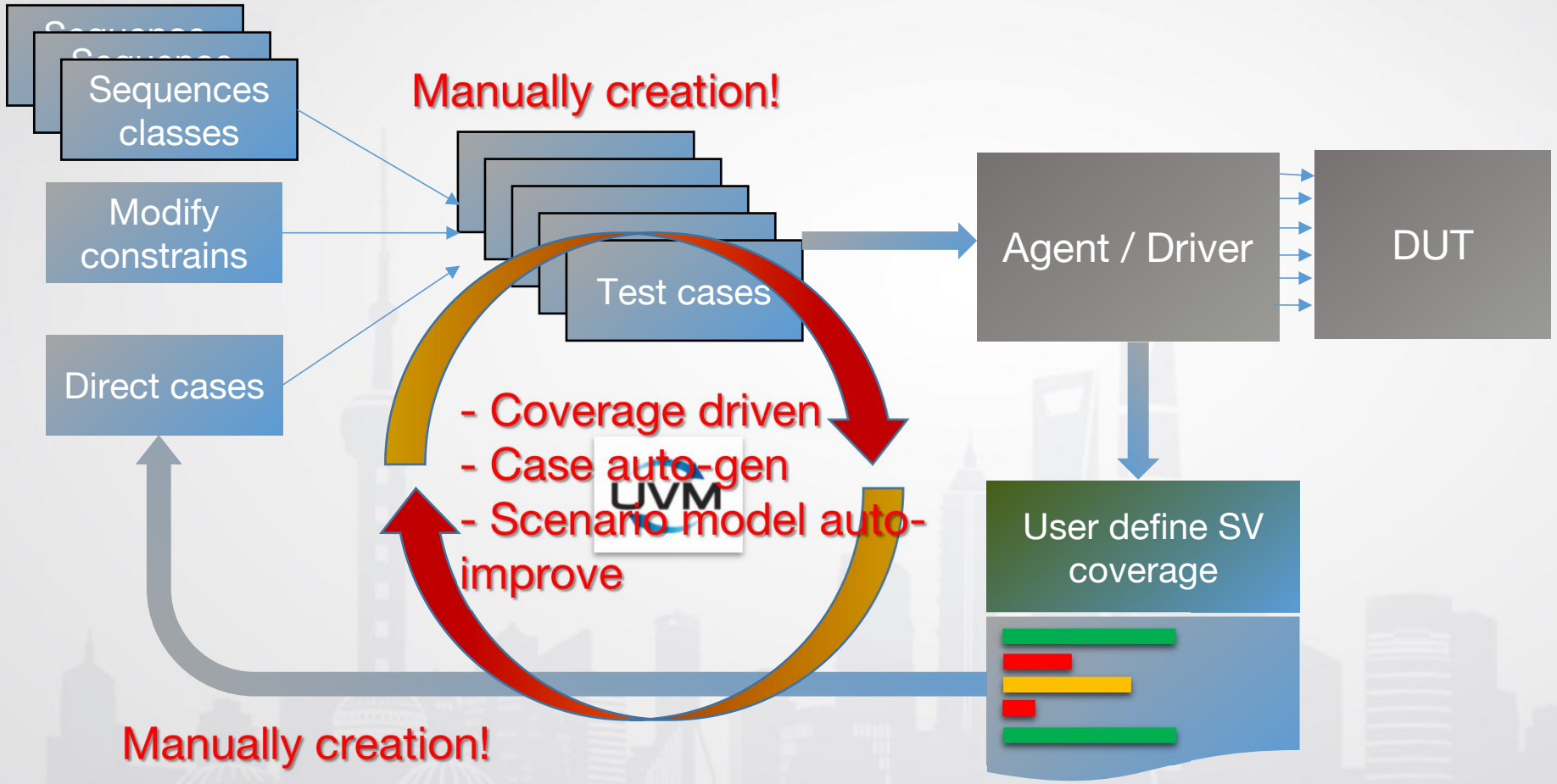
Key definition for descripting a verification scenario

- Collection (list, map, set, etc.)
- Operator expression
- Component action
- Activity control-flow construct
- Flow objects
- Resource object
- Algebraic constraint
- Coverage Spec construct
- Target template implementation
- Conditional code processing



传统验证迭代回归 – 如何打破?



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When Automotive FuSa Met IC

Jimmy Sun Technical Director from X-EPIC

Automotive Semiconductor

Question: How to switch my current IC to automotive version?

Answer: No. it is not reasonable.

Question: What should we do if we want to plan a automotive IC/IP?

Answer: at least, you should consider functional safety, reliability, Cyber Security and traceability.

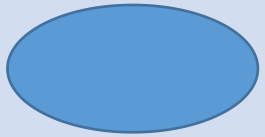
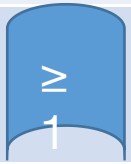
What is Functional Safety?
What is Functional Safety in semiconductor?

- Functional Safety in ISO 26262-1(Vocabulary)
  - Absence of unreasonable risk due to hazards caused by malfunctioning behaviour of E/E systems.
- Functional Safety in semiconductor
  - To avoid, detect and control systematic failure;
  - Perfect manufactory, reduce DPPM;
  - Detect and control random hardware failure;
- Safety Analysis Method
  - FTA
  - FMEA/FMEDA
  - DFA

In today's presentation, we will use FTA as an example to explain how to do Safety Analyses with FTA method in Semiconductor.

Fault Tree Analysis

- FTA is a top-down analysis method;
- FTA starts from top level failure mode to detect the root reason of failure;
- FTA is descripted by using symbols;

Symbol	Description
	Event
	And Gate, Probabilities should be P = P1 * P2
	Or Gate, Probabilities should be P = P1 + P2 – (P1*P2) ≈ P1 + P2
	Top or middle Event that should be analyzed

- Probability of Residual Failure:

$$P = \sum P_i$$

- Residual Failure Rate:

$$\lambda_{RF} = \sum \lambda_i$$

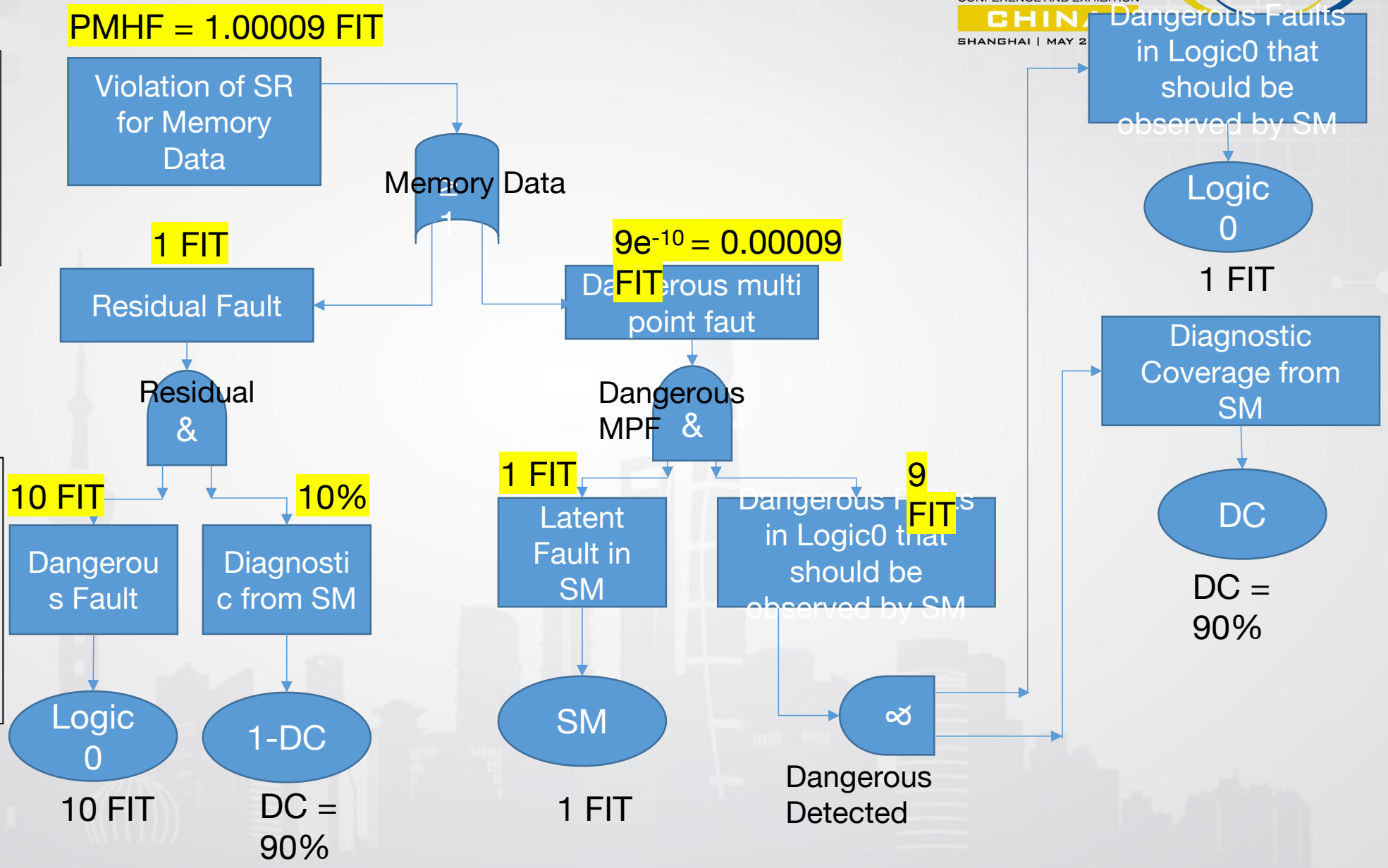
FTA Example for Semiconductor

Latent Fault:

1. SM failed;
2. Then Logic0 failed and SM can't detect it;

Assumptions:

- Logic0: 10 FIT
- SM: 1 FIT
- DC: 90%
- Runtime hours: 10000h



FTA Example for Semiconductor

PMHF = 1.00009 FIT

What we can do if PMHF didn't met target?

Solution:

- For Logc0 should reduce FIT number;
- For DC:
  - Improve SM to get high number DC;
  - Run fault injection to prove current SM has better DC: