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SYNOPSYS®

The New Power Perspective – Realistic Workloads – Real Results

Xiaoming Li, Synopsys

Agenda

- Why Power Matters
- Power Verification using Emulation
- Results

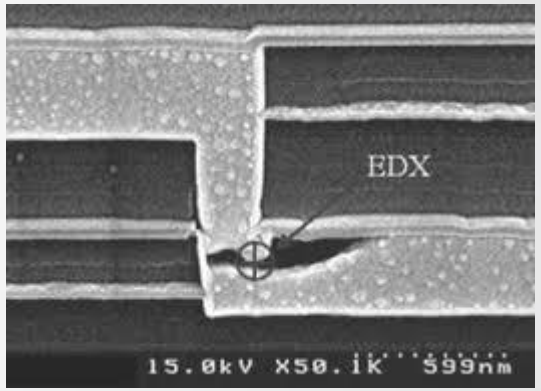
Power Consumption Drives Competitiveness

Peak and Average Power are Key Design Concerns

Battery life

Operational Cost

Packaging Cost



Reliability

Low Power Remains #1 Verification Issue

Synopsys Global User Survey 2020

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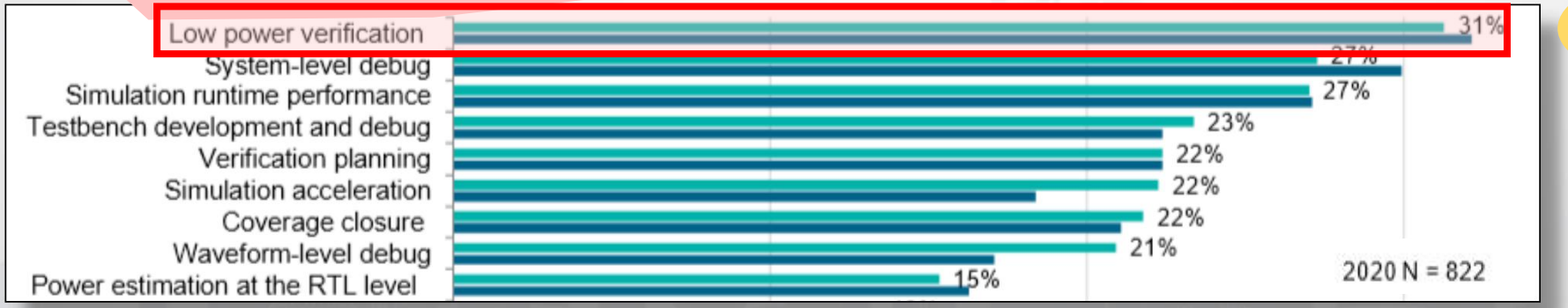
#1

14%

#1



31%

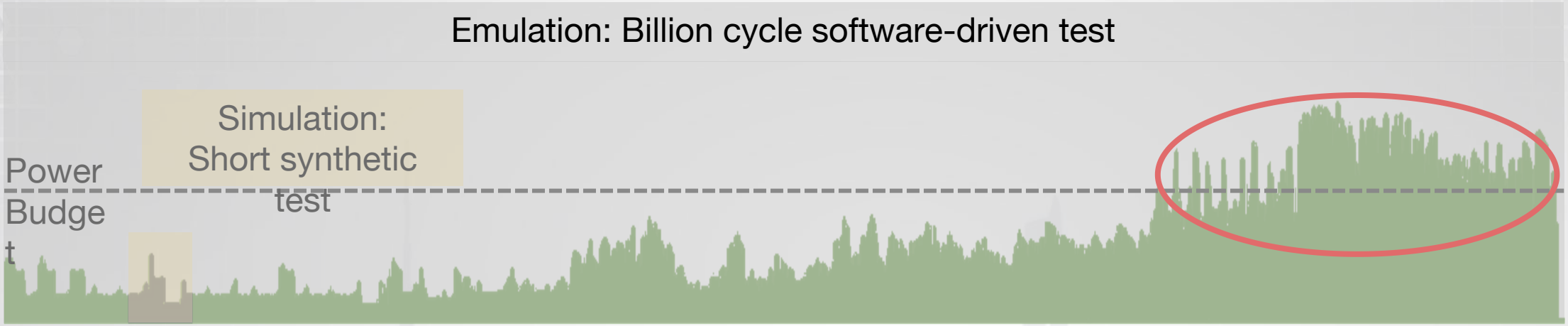
2020
2019
2018

2020 N = 1,214

Meeting Dynamic Power Requirements Becoming More Difficult

Peak Power Events Are Critical

Peak power events are driven by actual software workloads



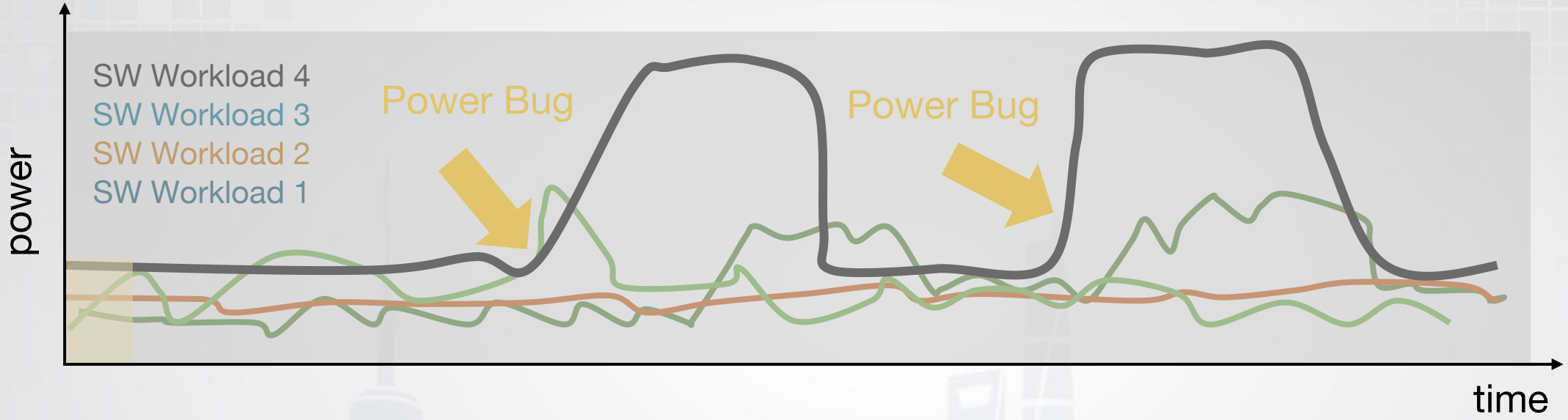
Peak power below budget
Signoff: OK

Actual peak above budget

Peak power above budget
Rework RTL before signoff

Actual chip peak power within expectations

Running SW Workloads to Find Power Bugs



Small tests do not expose realistic workload driven power bugs

Real firmware and OS are needed during pre-silicon testing

Must use emulation and verify power over millions or billions of cycles

Pre-silicon power verification enables debug not possible with actual silicon

How is Power Calculated?

Power Analysis Requires Waveforms, Technology Library and Signal Delay Data

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Total Power =

Logic Cell Power

- Switching Power: Capacity, Frequency, Voltage
- + Internal Power
- + Leakage Power

+ Clock Tree Power

+ Memory Power

Average Power

- Need # toggles, total duration at 0 and 1

Cycle Power

- 0-delay waveform for all signals for million cycles

Signoff Power

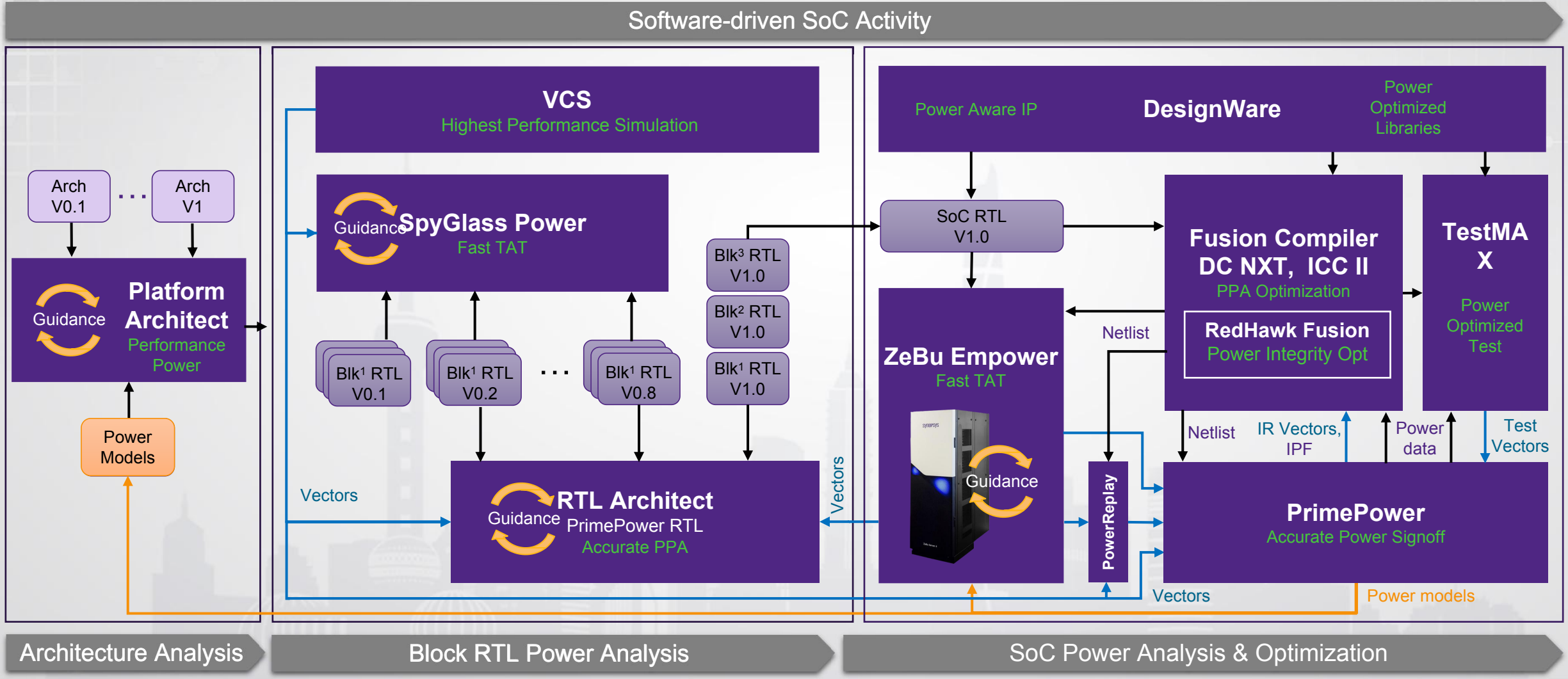
- Waveform for all signals with accurate delays

Data Formats

- SAIF: Switching Activity File
- .lib: Technology Library for Logic and Memory Internal and Leakage Power
- SPEF: Net Capacities File
- SDF: Net Delay File

Synopsys Software-Driven Low Power Solution

End-to-End low power solution from architecture to signoff



ZeBu Empower

Fastest Power Emulator for HW-SW Power Verification

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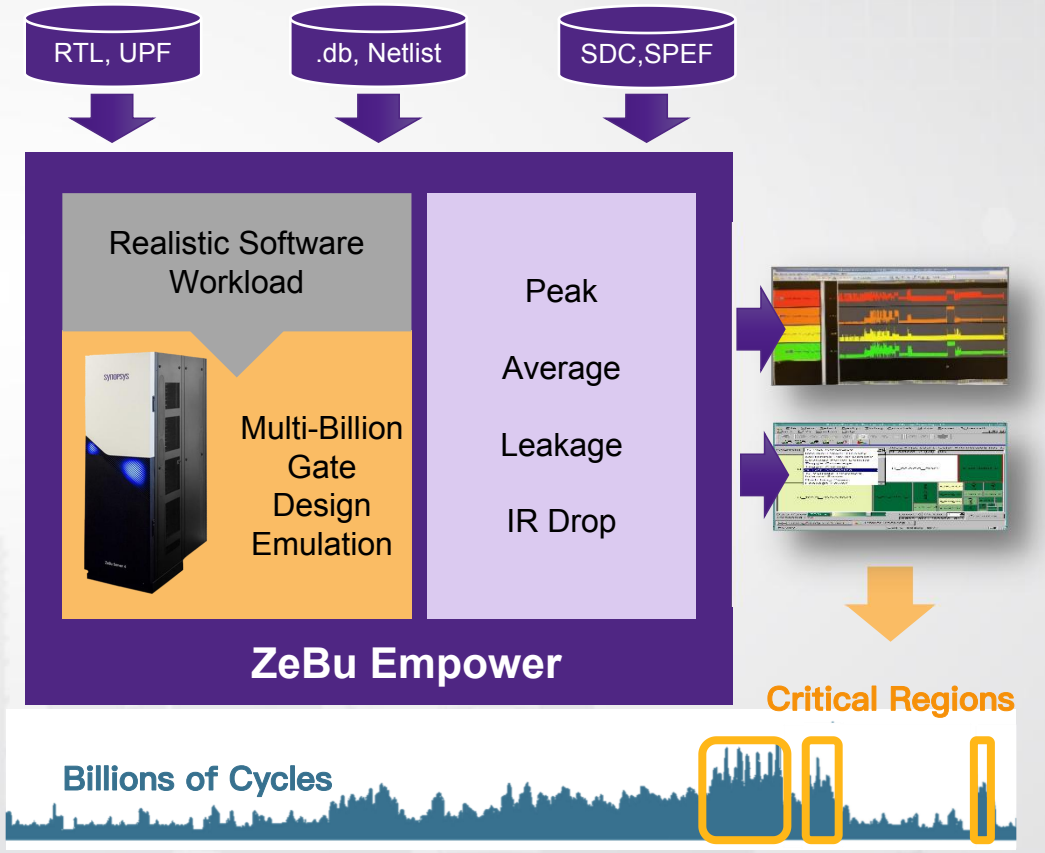
Key Benefits

Large designs, Realistic workloads,
Multiple iterations per day

Actionable power profiling for
dynamic and leakage power

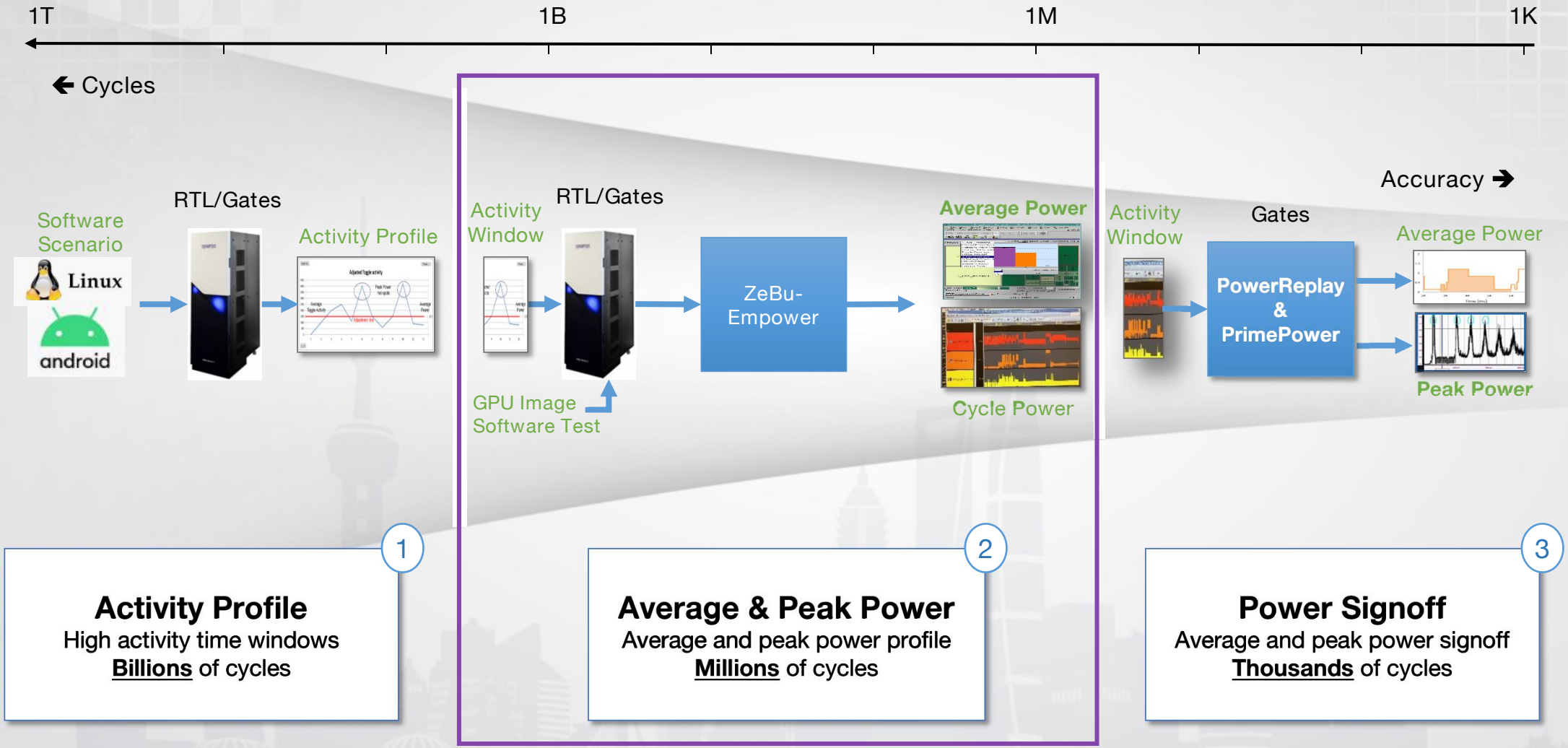
Power critical blocks and vectors
feeding into signoff analysis

Power Emulator



Hardware and Software Architected for Maximum Compute Throughput

Software-Driven SoC Power Analysis



Identify Peak Power with real stimulus: Zoom from billions cycles → Thousands of cycles

ZeBu Empower Power Analysis: RTL Cycle, RTL-2-Gate, Gate

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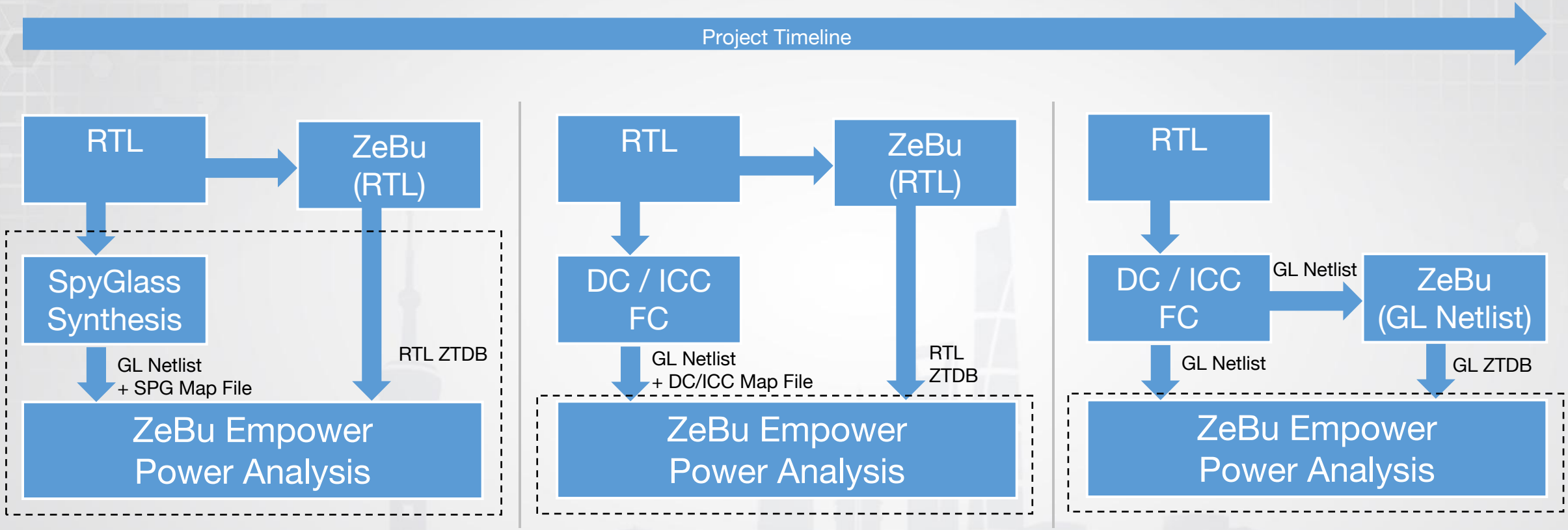

RTL Cycle Power

Early Power: Many Iterations, Fast TAT, Millions of cycles
Drives RTL / SW Changes

RTL-2-Gate Power

Early Netlist: Some iterations RTL ZeBu, Millions of cycles
Drives RTL / Layout changes

Pure Gate Power

Late Netlist: Few Iterations GL ZeBu, Millions of cycles
Drives Synth/Layout changes

ZeBu Empower Power Estimation: Tcl Shell & Average/Peak Power

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Flow Step	ZeBu Empower Command
Set all Required .dbs	`set link_library "tech.db mem.db"`
Read all Netlist Files	`read_verilog design.v; link`
Read Constraints	`read_sdc`
Read Parasitic Data	`read_parasitics dut.spef`
Read Activity File	`read_stimulus -file dut.ztdb`
Calculate Power	`compute_power`
Report Power	`report_power`

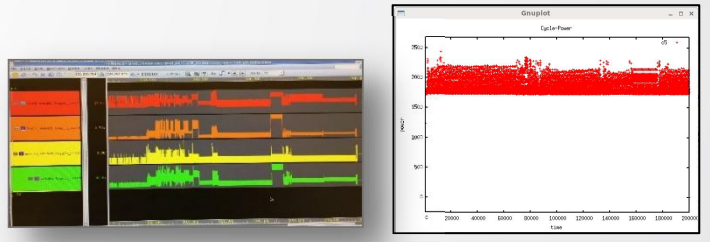
Standard Tcl Shell Commands
Compatible with PrimePower

Tcl Debug Shell
Debug design, Debug Power

```
                    Internal      Switching     Leakage       Total                    Peak          Peak
Power Group         Power         Power         Power         Power          (   %)    Power         Time
------------------------------------------------------------------------------------------------------------
-
clock_network       8.899e-04     0.000e+00     0.000e+00     8.899e-04     ( 48.18%)  8.901e-04     71640
register            9.527e-06     3.696e-06     3.760e-04     3.892e-04     ( 21.07%)  4.396e-04     77280
combinational       5.495e-05     4.844e-05     4.645e-04     5.679e-04     ( 30.75%)  1.114e-03     11280
sequential          0.000e+00     0.000e+00     0.000e+00     0.000e+00     (  0.00%)  0.000e+00     N/A
memory              0.000e+00     0.000e+00     0.000e+00     0.000e+00     (  0.00%)  0.000e+00     N/A
io_pad              0.000e+00     0.000e+00     0.000e+00     0.000e+00     (  0.00%)  0.000e+00     N/A
black_box           0.000e+00     0.000e+00     0.000e+00     0.000e+00     (  0.00%)  0.000e+00     N/A

  Net Switching Power  =    5.214e-05   (  2.82%)
  Cell Internal Power  =    9.544e-04   ( 51.67%)
  Cell Leakage Power   =    8.405e-04   ( 45.51%)
  Total Power          =    1.847e-03   (100.00%)

Peak Power             =    2.434e-03
Peak Time              =        11280
```



```
# WSH_TABLE_BEG
# name: or1200_cpu.pwave_cycle_power
# groups: /or1200_cpu
# cols_per_group: leakage internal switching total   <<- columns
# xunit: 1ns
# yunit: uW
# col_names: xkey=Time G1.C1 G1.C2 G1.C3 G1.C4
 100       8.304661e+02     3.958796e+02     6.054502e+00     1.232400e+03
 110       8.302657e+02     9.023951e+02     2.466496e+01     1.757326e+03
 120       8.300638e+02     9.084959e+02     3.577724e+01     1.774337e+03
 130       8.304145e+02     8.917342e+02     6.054502e+00     1.728203e+03
 140       8.301953e+02     9.040037e+02     2.506173e+01     1.759261e+03
```

Standard Tcl analysis shell, Average + Peak Power Reports

Read Parasitic Data / Net Annotation

wsh> report_parasitic_annotation

```
Info: Total 14,315 unique nets found, missing capacitance annotations 4(0.03%).
Info: Cap Unit: 0.001 pF, Data Source: SPEF(99.97%), WLM(0.03%)
Info: Wire cap stats: sum = 491.34, avg = 0.03, min = 0.54, max = 45.98
Info: Total cap stats: sum = 26008.90, avg = 1.82, min = 0.00, max = 1373.96
Info: SPEF Annotation Summary
```

Nets Driven by	Annotated (%)	Not Annotated Loadless (%)	Not Annotated Loaded (%)	Total
Primary Input	385(99.74%)	0(0%)	1(0.26%)	386
IO Pads	0(0%)	0(0%)	0(0%)	0
Black Box	0(0%)	0(0%)	0(0%)	0
Memory	0(0%)	0(0%)	0(0%)	0
Register	2,943(99.97%)	0(0%)	1(0.03%)	2,944
Latch	0(0%)	0(0%)	0(0%)	0
Other Sequential	0(0%)	0(0%)	0(0%)	0
Clock Gate	0(0%)	0(0%)	0(0%)	0
Combinational	10,983(99.98%)	0(0%)	2(0.02%)	10,985
	14,311(99.97%)	0(0%)	4(0.03%)	14,315

All nets: primary Input, Register, Combinational… Goal 0% Not Annotated – if not debug…

Read Stimulus / Net Annotation


```
wsh> report_activity_annotation -list_not_annotated

Info: Processing -root /or1200_cpu, -stim_id /wsdb/stim1 ...
Info: Activity Annotation: -root /or1200_cpu, -stim_id /wsdb/stim1
Info: Checking for drivers with missing waveform annotations.
Info: Total 2,277 essential drivers found, missing waveforms 0(0%).
      BEG: Waveform Annotation Summary
      ------------------------------------------------------------------------------------------
                         From Activity     From                Not Annotated     Not Annotated
      Nets Driven by     File (%)          Constants (%)       Loadless (%)      Loaded (%)        Total (%)
      ------------------------------------------------------------------------------------------
      Primary Input      386(99.48%)       0(0%)               2(0.52%)          0(0%)             388(17.03%)
      IO Pads            0(0%)             0(0%)               0(0%)             0(0%)             0(0%)
      Black Box          0(0%)             0(0%)               0(0%)             0(0%)             0(0%)
      Memory             0(0%)             0(0%)               0(0%)             0(0%)             0(0%)
      Register           1,891(100%)       0(0%)               0(0%)             0(0%)             1,891(82.97%)
      Latch              0(0%)             0(0%)               0(0%)             0(0%)             0(0%)
      Other Sequential   0(0%)             0(0%)               0(0%)             0(0%)             0(0%)
      Clock Gate         0(0%)             0(0%)               0(0%)             0(0%)             0(0%)
      Combinational      0(0%)             0(0%)               0(0%)             0(0%)             0(0%)
      Empty Modules      0(0%)             0(0%)               0(0%)             0(0%)             0(0%)
      ------------------------------------------------------------------------------------------
                         2,277(99.91%)     0(0%)               2(0.09%)          0(0%)             2,279(100%)
      ------------------------------------------------------------------------------------------
Info: Detailed annotation report saved in: wsh_work/or1200_cpu.stim1.annotation.rpt
```

Essential Signals: Sequential Outputs, Memory Outputs, Port Inputs (not combos). Goal 0% Not Annotated – if not debug…

Computer Power/ Cell Computed

```
info: Total cells:                    12,192
Info: Total computed cells:           12,192(100%)
Info: Power Computation Summary
      ------------------------------------------------------------------
                     Power                  Power
      Power Group    Computed (%)           Not Computed (%)    Total
      ------------------------------------------------------------------
      clock_network  0(0%)                  0(0%)               0
      register       1,891(100%)            0(0%)               1,891
      combinational  10,301(100%)           0(0%)               10,301
      sequential     0(0%)                  0(0%)               0
      memory         0(0%)                  0(0%)               0
      io_pad         0(0%)                  0(0%)               0
      black_box      0(0%)                  0(0%)               0
      ------------------------------------------------------------------
                     12,192(100%)           0(0%)               12,192
      ------------------------------------------------------------------
```

All cells: clock_network, register, combinational, memory... Goal 0% Not Computed – if not debug…

Local Customer Use Case

Bring-up Effort

- Flow is rather simple and clear
- PrimePower script can be easily reused
- Generally one day set-up period for new project

Speed

- Typical TAT is around ~2 hours for tens of millions gate counts design
- Typical TAT is around ~12 hours for hundreds of millions gate counts design
- Native PC farm support, more farm resource, less TAT
- Multi-iterations per day

It is the first time to perform complex power analysis with real software workload at pre-silicon stage for millions of cycles, including DFS, clock gating feature enabled.

Local Customer Use Case

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Average power <2% deviation compared with PrimePower

PrimePower

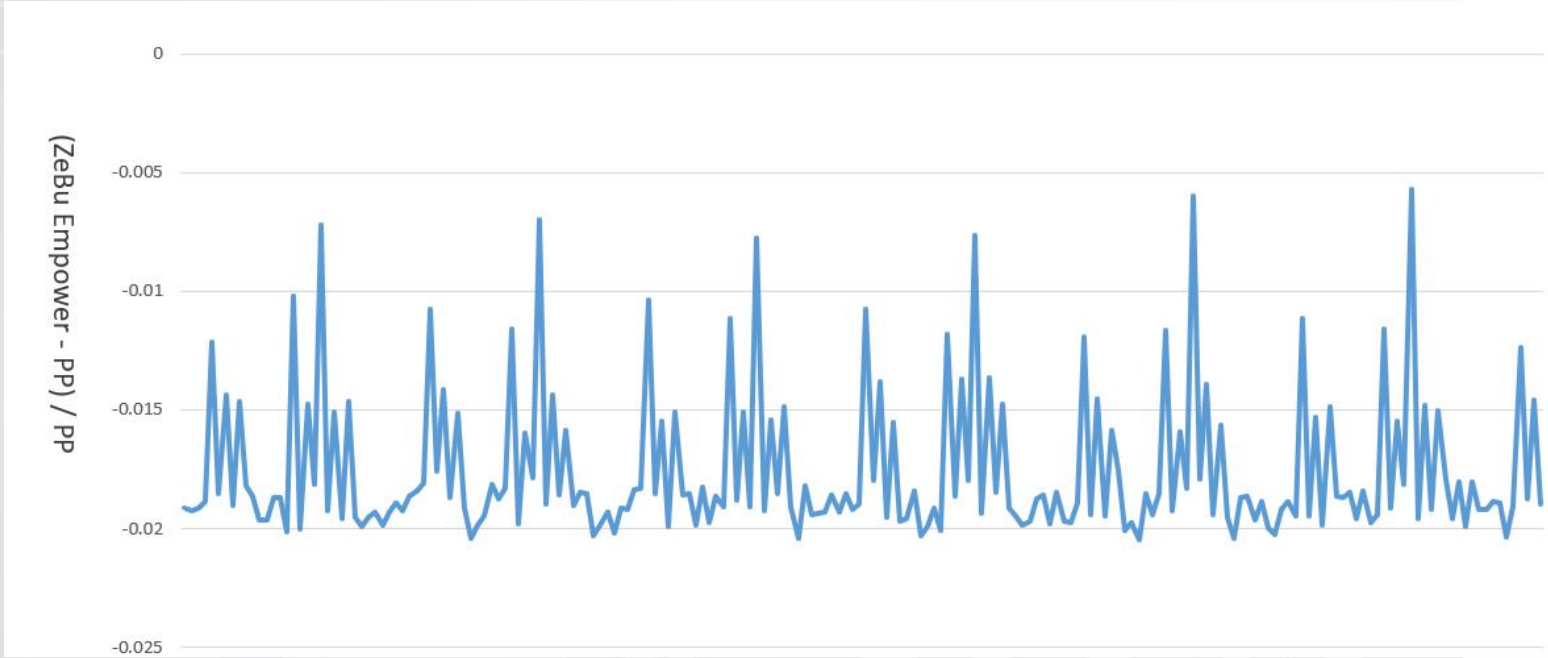
```
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                          Internal  Switching  Leakage     Total
Power Group               Power     Power      Power       Power   (     %)  Attrs
------------------------------------------------------------------------------------
clock_network               2.0498    0.4879     0.0175     2.5552 (63.55%)  i
register                 3.709e-03 4.484e-03     0.1036     0.1118 ( 2.78%)
combinational            3.798e-03 9.097e-03     0.2764     0.2893 ( 7.20%)
sequential                  0.0000    0.0000 3.689e-04  3.689e-04 ( 0.01%)
memory                      0.9287 6.761e-08     0.1353     1.0641 (26.46%)
io_pad                      0.0000    0.0000     0.0000     0.0000 ( 0.00%)
black_box                   0.0000    0.0000     0.0000     0.0000 ( 0.00%)

  Net Switching Power  =     0.5015   (12.47%)
  Cell Internal Power  =     2.9861   (74.27%)
  Cell Leakage Power   =     0.5332   (13.26%)
                         ---------
Total Power            =     4.0208  (100.00%)
```

ZeBu Empower

```
 9  Attributes
10  ----------
11      i  -  Including register clock pin internal power
12      u  -  User defined power group
13
14                        Internal     Switching    Leakage      Total                  Peak         Peak
15 Power Group            Power        Power        Power        Power        (     %)  Power        Time          Attrs
16 ------------------------------------------------------------------------------------------------------------------
17 clock_network          2.027e+00    4.867e-01    1.758e-02    2.531e+00    ( 63.37%)  3.588e+00    180459561.984 i
18 register               3.697e-03    4.472e-03    1.041e-01    1.122e-01    (  2.81%)  1.250e-01    180459596.616
19 combinational          3.810e-03    9.084e-03    2.764e-01    2.893e-01    (  7.24%)  3.085e-01    180459575.088
20 sequential             4.498e-06    2.558e-07    1.101e-05    1.577e-05    (  0.00%)  2.044e-05    180459569.472
21 memory                 9.264e-01    6.744e-08    1.353e-01    1.062e+00    ( 26.58%)  1.701e+00    180459563.856
22 io_pad                 0.000e+00    0.000e+00    0.000e+00    0.000e+00    (  0.00%)  0.000e+00    N/A
23 black_box              0.000e+00    0.000e+00    0.000e+00    0.000e+00    (  0.00%)  0.000e+00    N/A
24
25   Net Switching Power  =    5.002e-01   ( 12.52%)
26   Cell Internal Power  =    2.961e+00   ( 74.12%)
27   Cell Leakage Power   =    5.334e-01   ( 13.35%)
28                          ------------
29 Total Power            =    3.994e+00  (100.00%)
30
```

Local Customer Use Case

Cycle power <5% deviation compared with PrimePower



PP (W)	ZeBu Empower (W)	(ZeBu Empower - PP)/PP
4.53	4.44	-0.01911766
4.53	4.44	-0.019269536
4.56	4.47	-0.019126535
4.53	4.44	-0.01888543
4.56	4.50	-0.012141009
4.57	4.49	-0.01855186
4.56	4.49	-0.014354386
4.55	4.46	-0.019007692
4.55	4.48	-0.014616044
4.55	4.47	-0.018207253
4.56	4.47	-0.018641009
4.54	4.45	-0.019657489
4.53	4.44	-0.019637307
4.53	4.45	-0.018675055
4.53	4.45	-0.018703753
4.53	4.44	-0.020122737
4.52	4.47	-0.010213938
4.53	4.44	-0.02002362
4.56	4.49	-0.014760965
4.53	4.45	-0.018122958
4.54	4.51	-0.007194053
4.56	4.47	-0.019219737
4.55	4.48	-0.015076264
4.54	4.45	-0.019574449
4.55	4.48	-0.014661758
4.55	4.46	-0.019503077
4.56	4.47	-0.019928289

ZeBu Empower - Multiple Turns per Day

3h TAT – Daily TAT not possible before GPU Design, 5M Cycles, 4.8MG, 8 CPUs	Major US Processor Company
12h TAT – Not possible before AI Design, 1.5M Cycles, 300MG, 150 CPUs	China AI Startup
1.1h TAT - Using only 14GB/CPU GPU Design, 2.6M Cycles, 5MG, 24 CPUs	Major US Processor Company
2h TAT – Good QoR for Exploration GPU Design, 0.7M Cycles, 28MG, 8 CPUs	Leading IP Provider

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