2021 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA
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accellera SYSTEMS INITIATIVE

Sequential Equivalence Check beyond Clock Gating Verification

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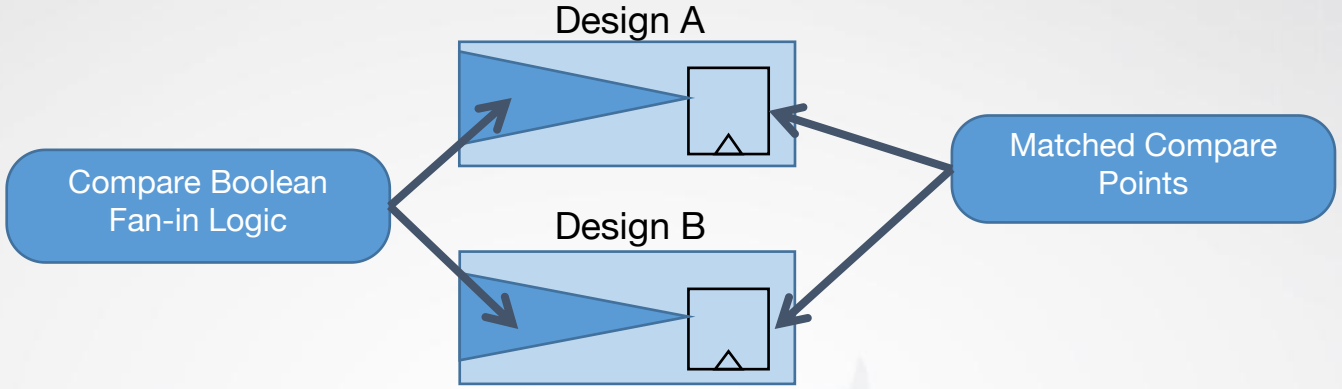
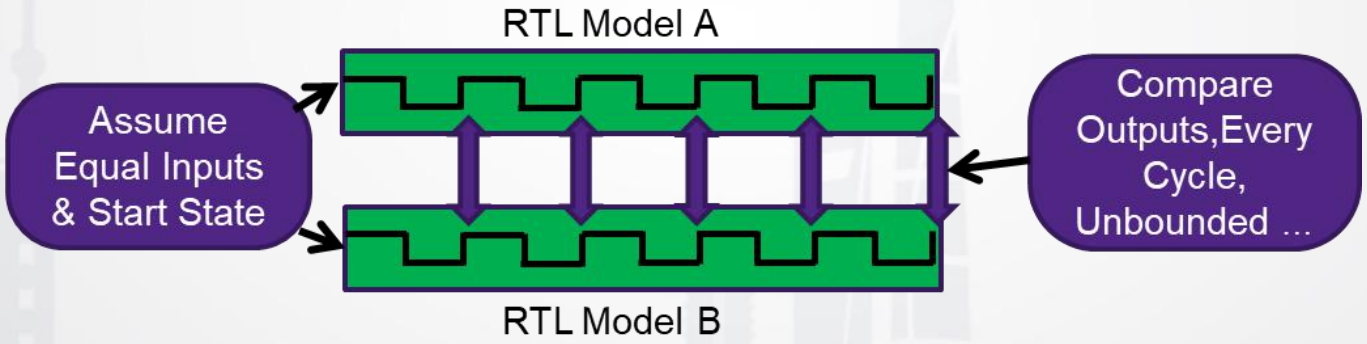
Different Types of Equivalence Checking

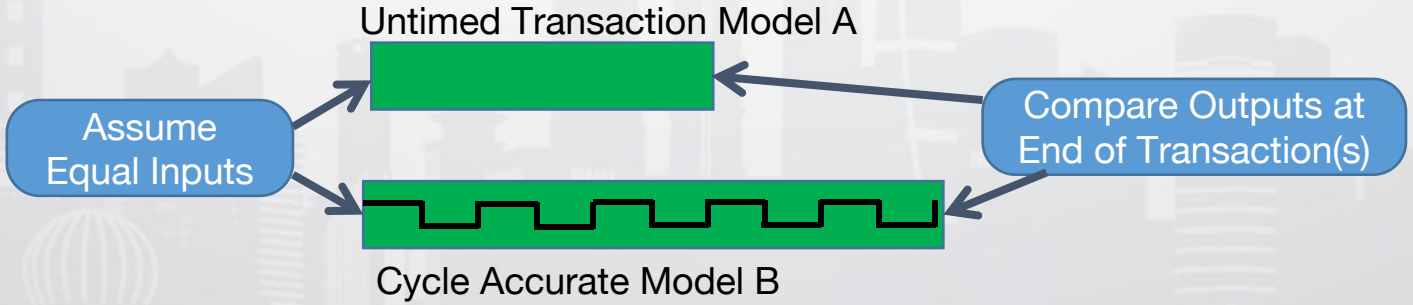
Boolean Equivalence (Formality)



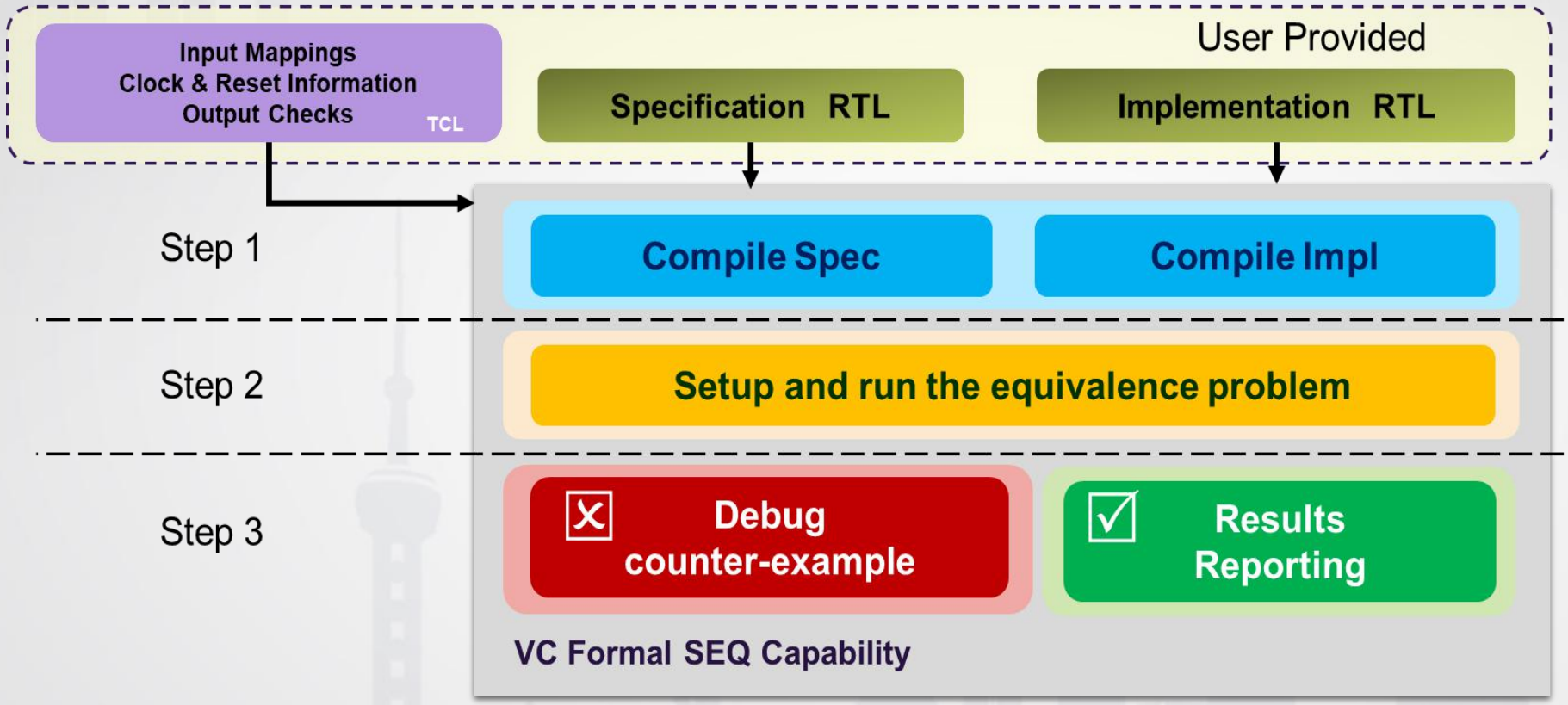
Sequential Equivalence (SEQ)



Transaction Equivalence (DPV)



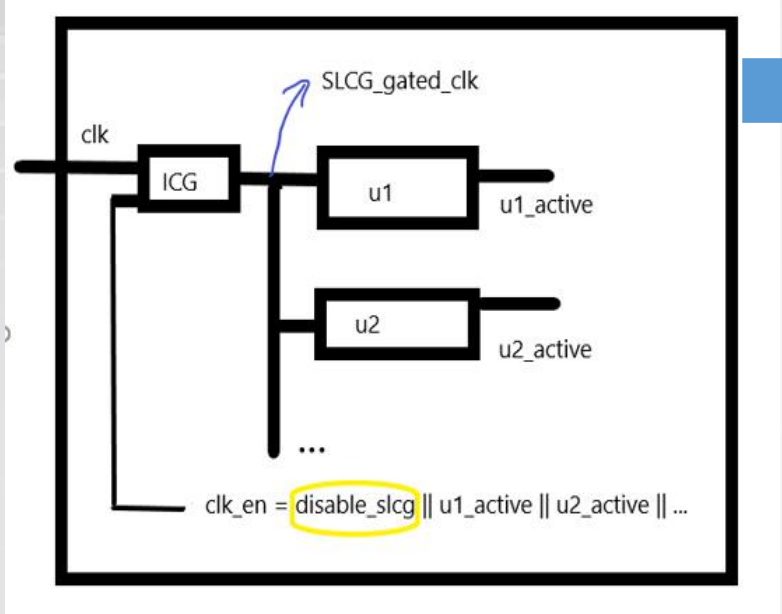
Sequential Equivalence Setup



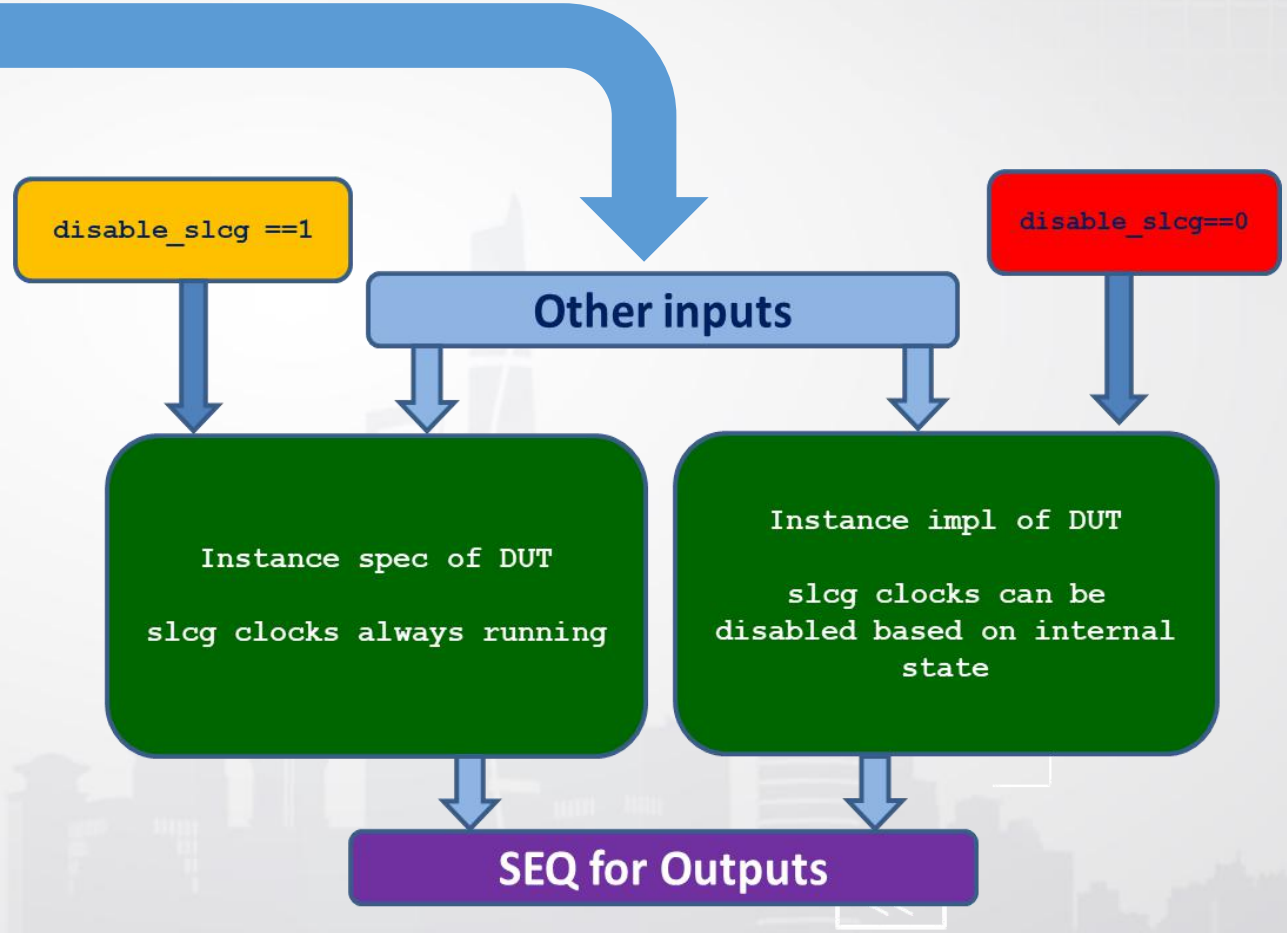
Two designs that produce same output on every clock cycle from valid initial states given the same inputs are sequentially equivalent.

Clock-Gating Verification

Clock gated design



Task: Ensure no output mismatch for all possible legal input combinations



SEQ Applications beyond Clock Gating

1. Verify RTL de-feature

```
input feature_foo_input_vld;
…
`ifdef enable_feature_foo
assign foo = ….;
…
`else
assign foo = 0;
…
`endif
```

SPEC:
+define+enable_feature_foo
fvassume feature_foo_input_vld==0

IMPL

2. Verify RTL add-feature

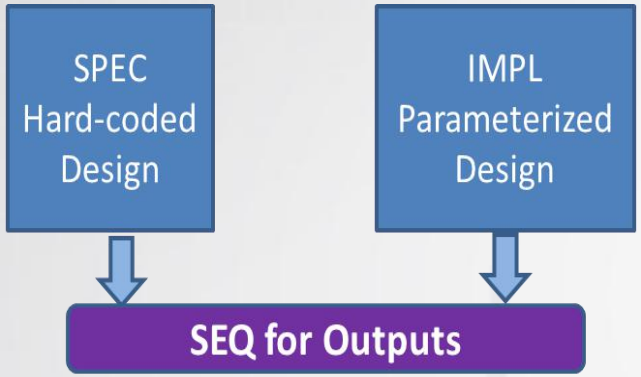
```
…
`ifdef new_feature_foo
assign foo = ….;
`endif
…
```

SPEC
Without define+new_feature_foo

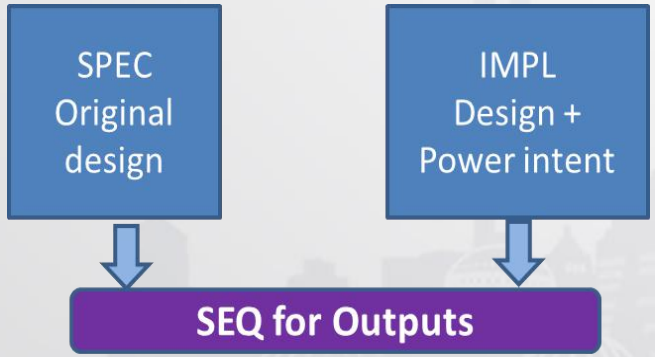
IMPL

SEQ Applications beyond Clock Gating

3. Verify parameterized design changes

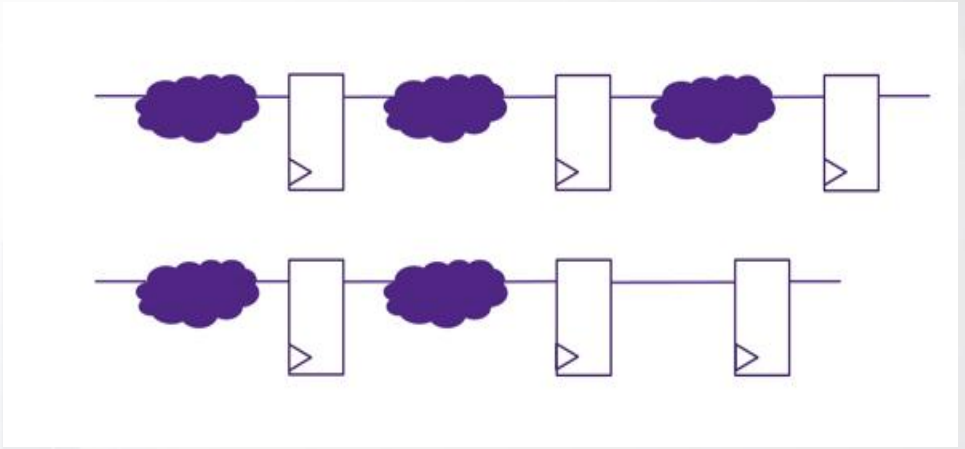


4. Verify design changes due to power



5. Verify designs with timing changes

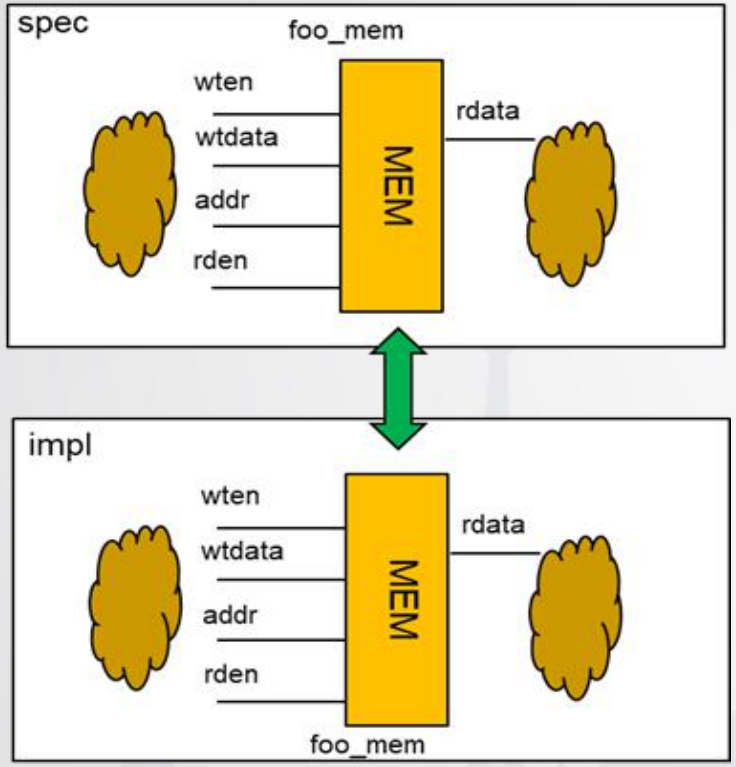
- Swap building cells, memory cells, clock gating cells
- Shorten pipeline stages



- Move logic across flop boundaries for timing

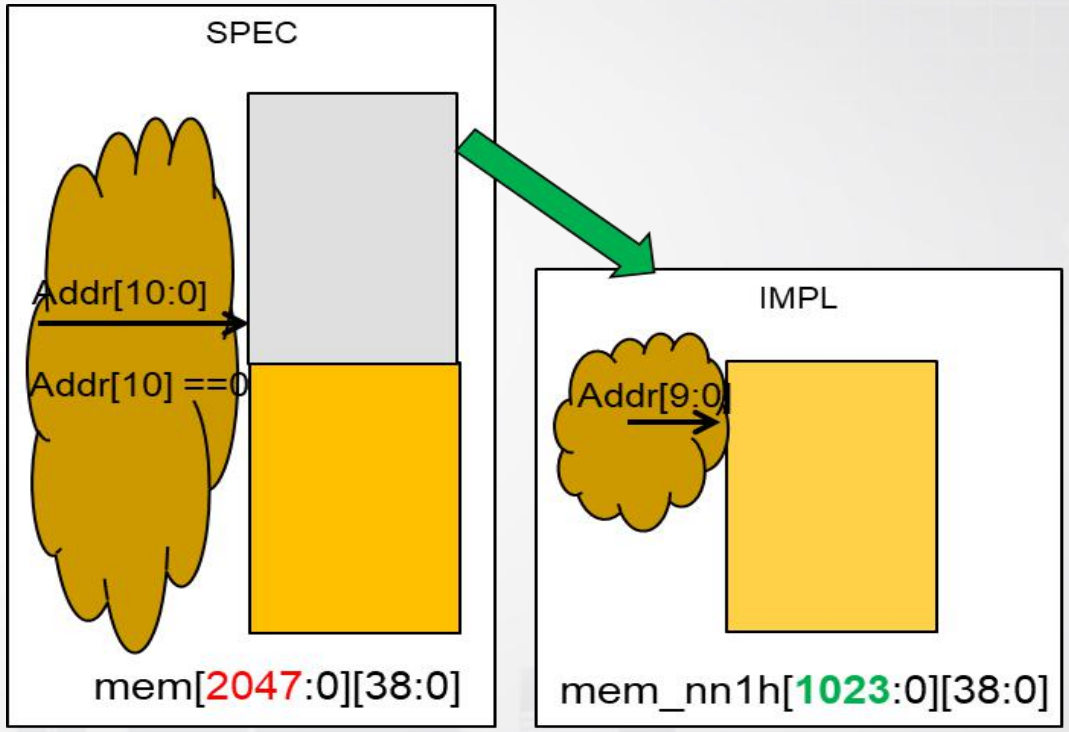
Convergence Techniques

- Redefine equivalence for accuracy



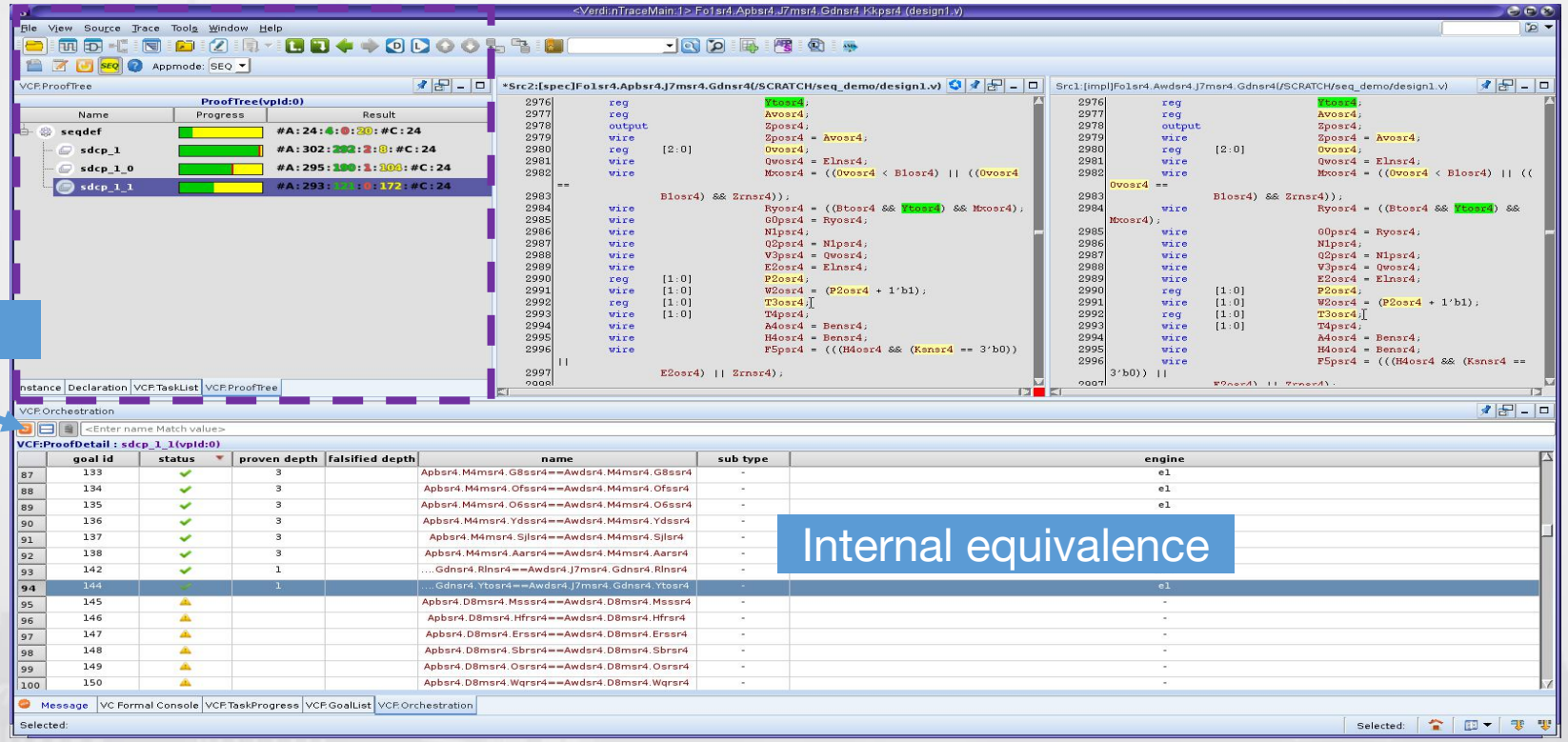
Blackbox, snip driver

- Partial word mapping



Orchestration view

- Convergence Debug Aid – Orchestration View
  - Highlights progress for ongoing refinement steps
  - Failures in the child proofs do not automatically mean failure in any of its parent-proof's

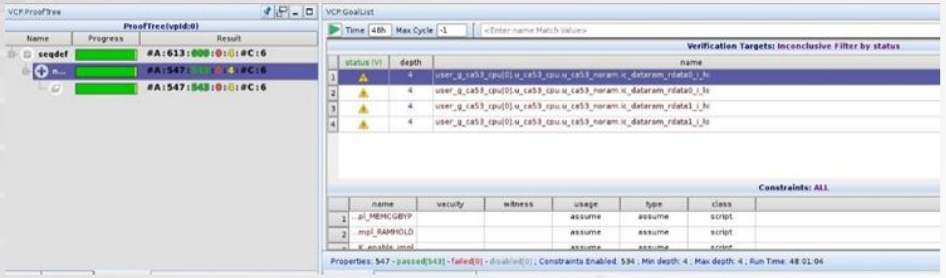


Report and Control Register Mappings

- "report_seq_mappings" provide information on
  - All the mapping points
  - All the points not mapped
- Internal mappings have significant impact on the convergence

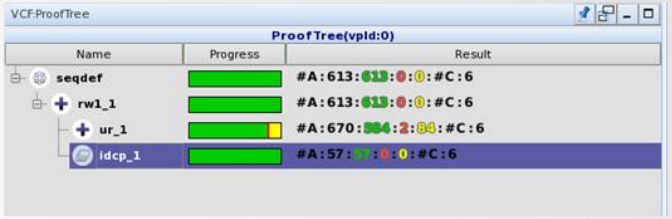
```
vcf> report_seq_mappings -backend
-------------------------------------------------------
Intial register mappings found based on name matching.
 - Note these are hints and not assumed to hold.
-------------------------------------------------------
[Mapped]                  - impl.go1(1) == spec.go1(1)
[Mapped]                  - impl.go2(1) == spec.go2(1)
[Mapped]                  - impl.go3(1) == spec.go3(1)
[Mapped]                  - impl.go4(1) == spec.go4(1)
[Mapped]                  - impl.product(16) == spec.product(16)
[Mapped]                  - impl.stage1(16) == spec.stage1(16)
[Mapped]                  - impl.stage2(32) == spec.stage2(32)
[Mapped]                  - impl.stage3(32) == spec.stage3(32)
[Mapped]                  - impl.stage4(24) == spec.stage4(24)
[Mapped]                  - impl.valid(1) == spec.valid(1)
[Not Mapped] - Not Found - impl.cg2.en_out(1)
[Not Mapped] - Not Found - impl.cg3.en_out(1)
[Not Mapped] - Not Found - impl.cg4.en_out(1)
-------------------------------------------------------
Total (Mapped 10) (Not mapped 3)
1
```

Results



4 inconclusive after 3 days

partial word mapping
seqmap internal mapping



Full proof within 2 hours