

Sequential Equivalence Check beyond Clock Gating Verification

Xiushan Feng, Samsung

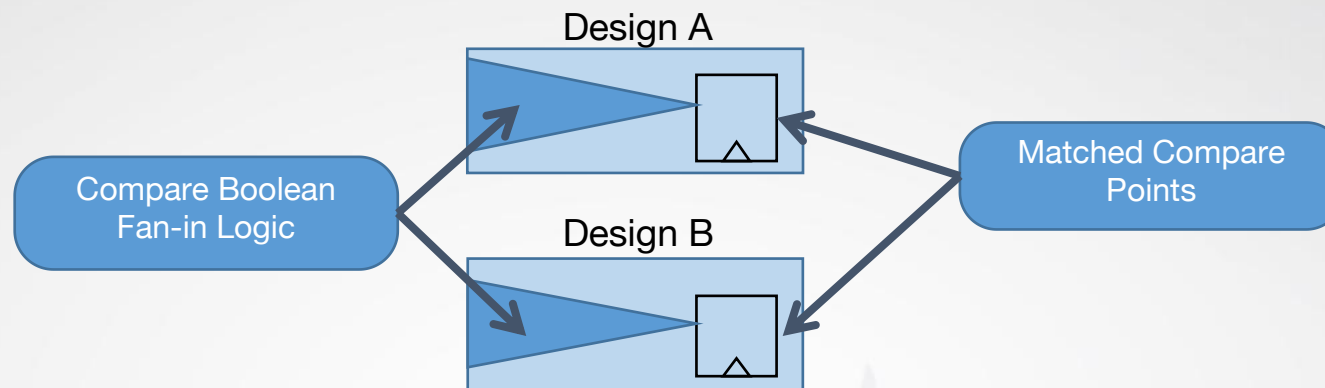
Xiaolin Chen, Synopsys

Sarah Li, Synopsys

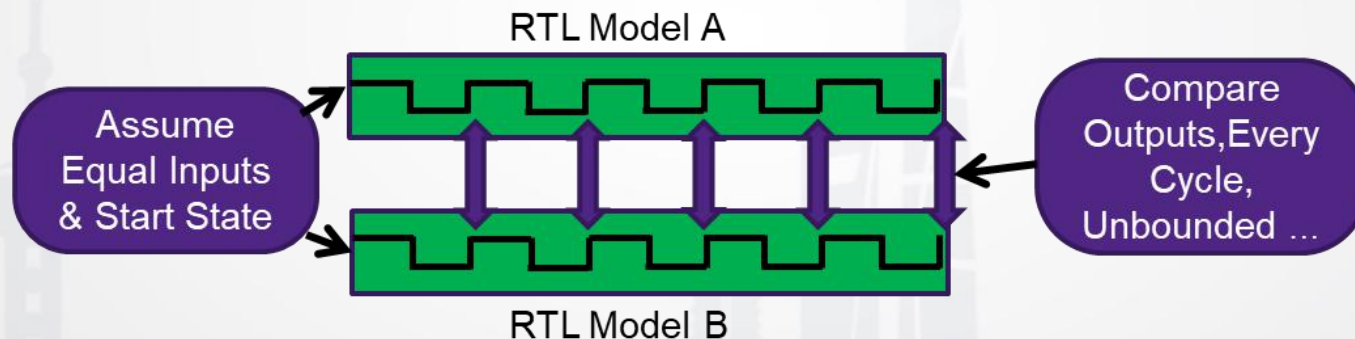


Different Types of Equivalence Checking

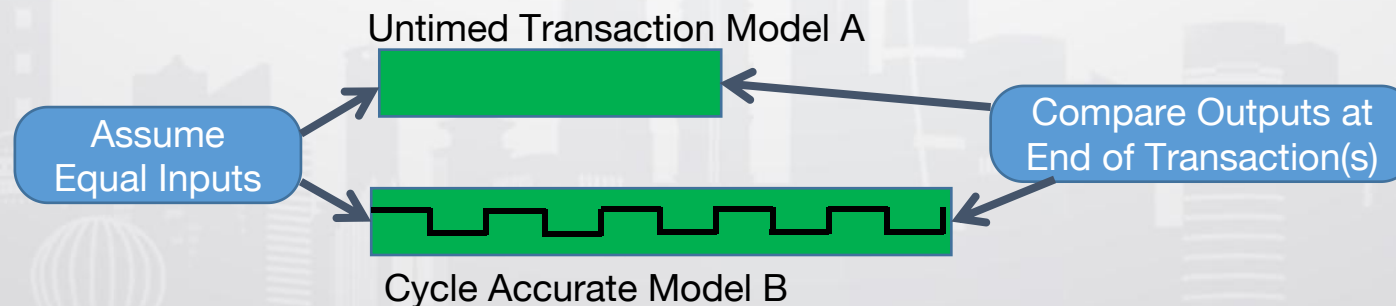
Boolean Equivalence (Formality)



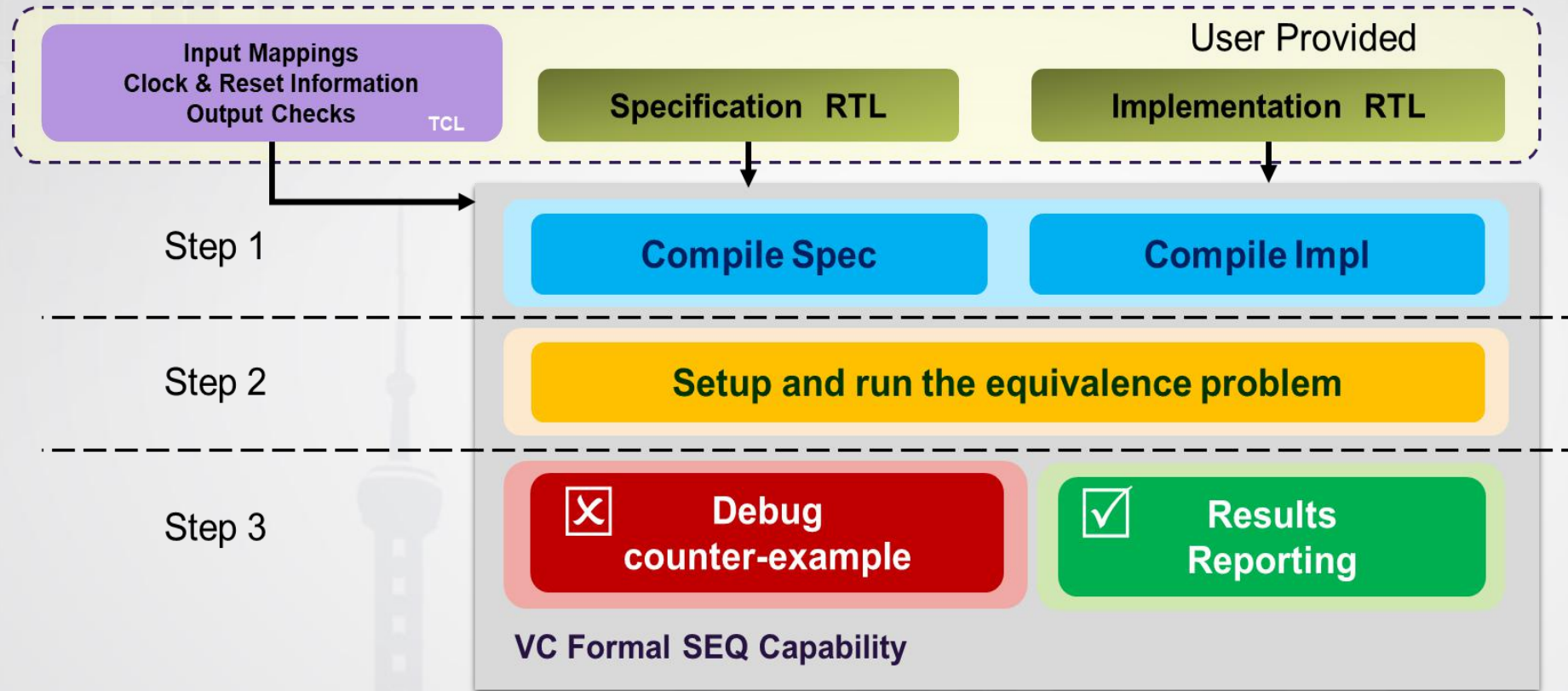
Sequential Equivalence (SEQ)



Transaction Equivalence (DPV)



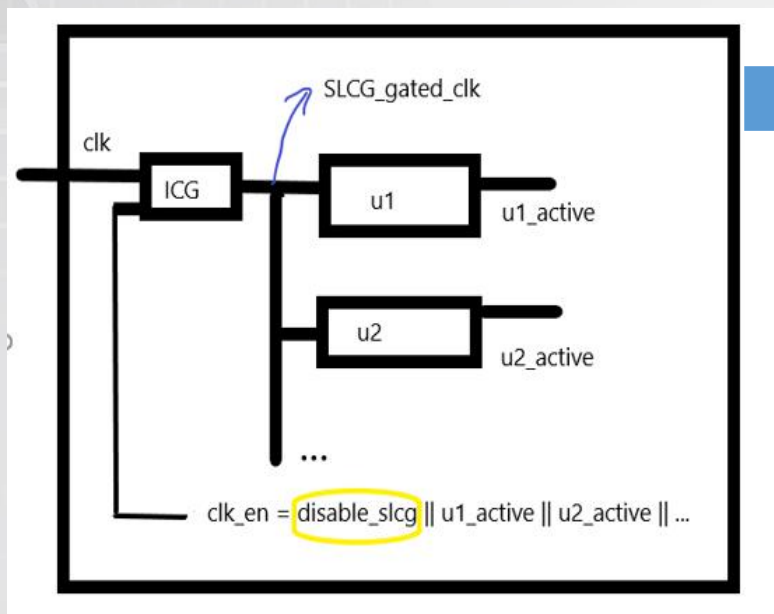
Sequential Equivalence Setup



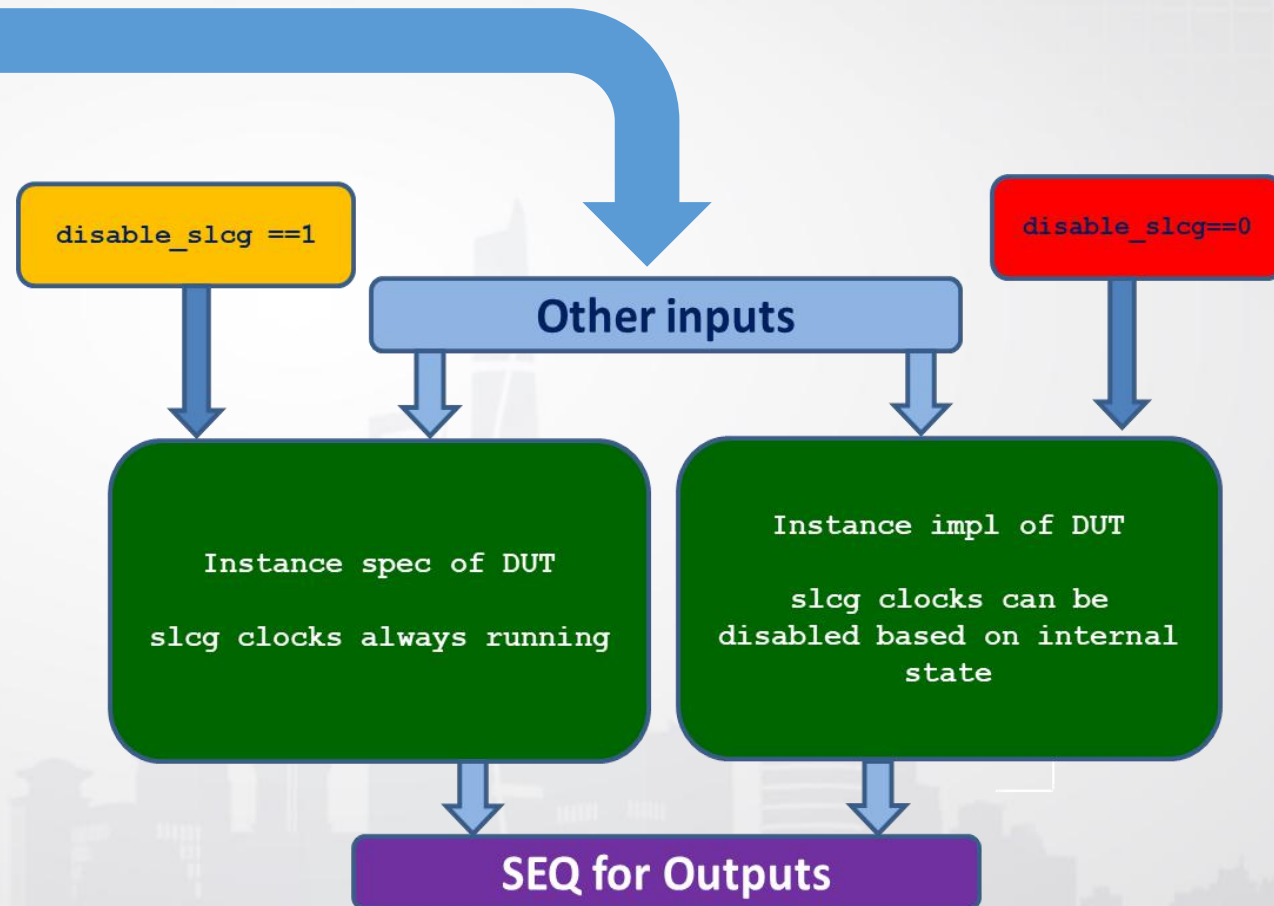
Two designs that produce same output on **every clock cycle** from valid initial states given the same inputs are sequentially equivalent.

Clock-Gating Verification

Clock gated design



Task: Ensure no output mismatch for all possible legal input combinations



SEQ Applications beyond Clock Gating

1. Verify RTL de-feature

```
input feature_foo_input_vld;  
...  
`ifdef enable_feature_foo  
assign foo = ....;  
...  
`else  
assign foo = 0;  
...  
`endif
```

SPEC:
+define+enable_feature_foo
fvassume feature_foo_input_vld==0



IMPL

2. Verify RTL add-feature

```
...  
`ifdef new_feature_foo  
assign foo = ....;  
`endif  
...
```

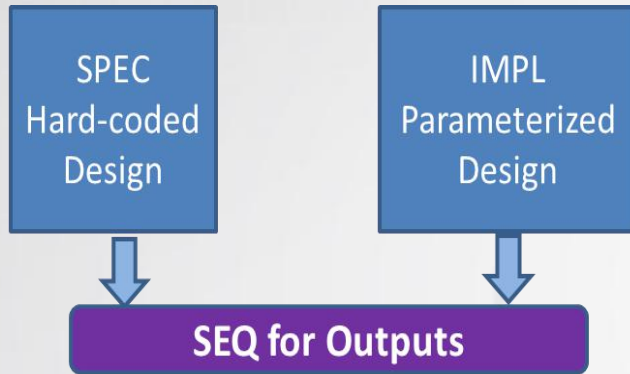
SPEC
Without define+new_feature_foo



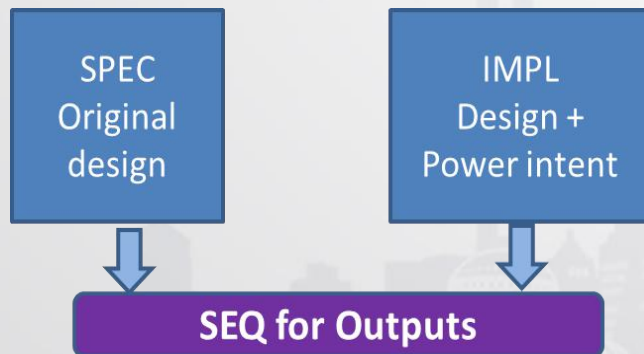
IMPL

SEQ Applications beyond Clock Gating

3. Verify parameterized design changes

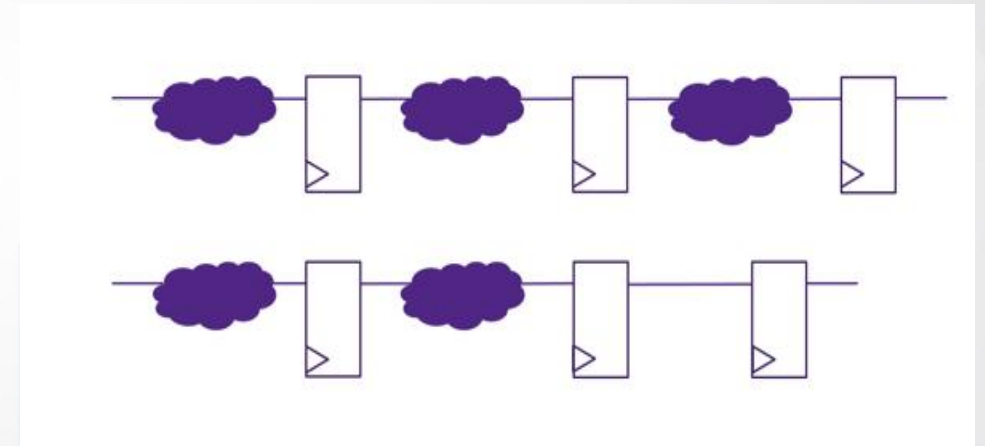


4. Verify design changes due to power



5. Verify designs with timing changes

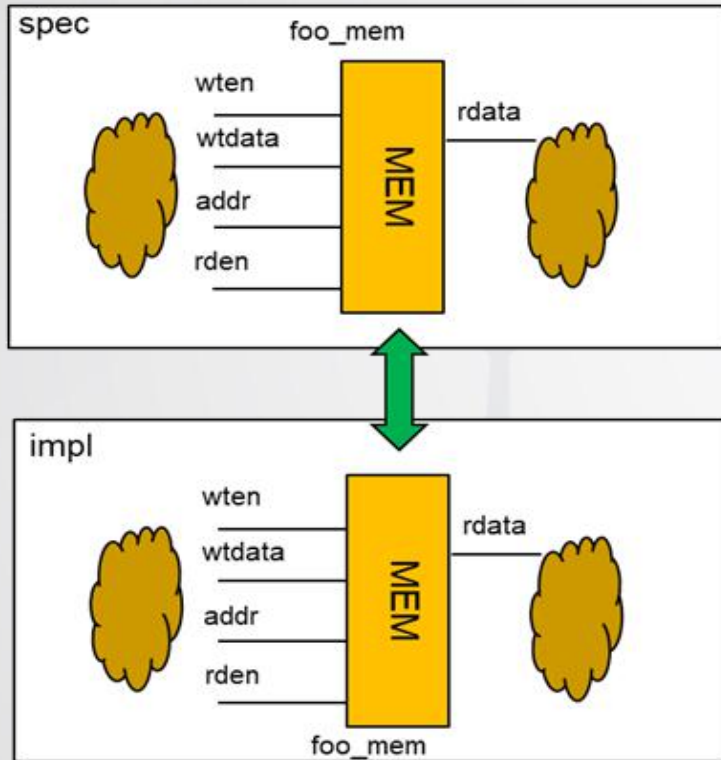
- Swap building cells, memory cells, clock gating cells
- Shorten pipeline stages



- Move logic across flop boundaries for timing

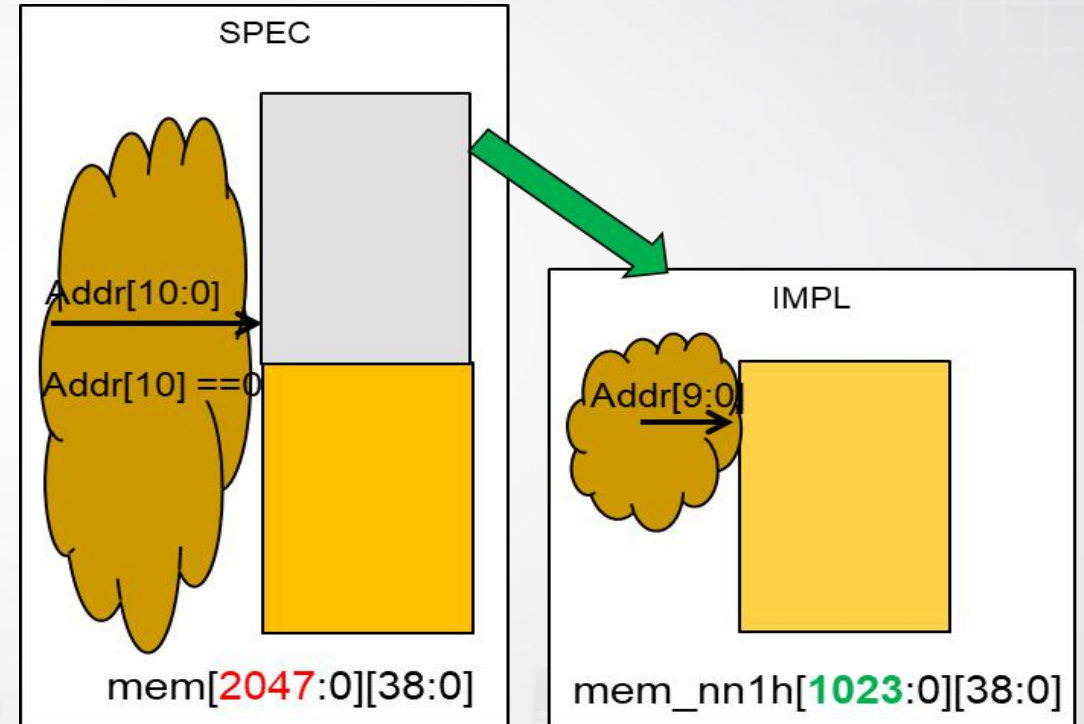
Convergence Techniques

- Redefine equivalence for accuracy



Blackbox, snip driver

- Partial word mapping



Orchestration view

- Convergence Debug Aid – Orchestration View
 - Highlights progress for ongoing refinement steps
 - Failures in the child proofs do not automatically mean failure in any of its parent-proof's

Highlighting source

Internal equivalence

goal id	status	proven depth	falsified depth	name	sub type	engine
87	133	3		Apbsr4.M4msr4.G8ssr4==Awdsr4.M4msr4.G8ssr4	-	el
88	134	3		Apbsr4.M4msr4.Ofssr4==Awdsr4.M4msr4.Ofssr4	-	el
89	135	3		Apbsr4.M4msr4.O6ssr4==Awdsr4.M4msr4.O6ssr4	-	el
90	136	3		Apbsr4.M4msr4.Ydssr4==Awdsr4.M4msr4.Ydssr4	-	-
91	137	3		Apbsr4.M4msr4.Sjlsr4==Awdsr4.M4msr4.Sjlsr4	-	-
92	138	3		Apbsr4.M4msr4.Aarsr4==Awdsr4.M4msr4.Aarsr4	-	-
93	142	1		...Gdmsr4.Rlnsr4==Awdsr4.J7msr4.Gdmsr4.Rlnsr4	-	-
94	144	1		...Gdmsr4.Ytosr4==Awdsr4.J7msr4.Gdmsr4.Ytosr4	-	el
95	145			Apbsr4.D8msr4.Msssr4==Awdsr4.D8msr4.Msssr4	-	-
96	146			Apbsr4.D8msr4.Hfrsr4==Awdsr4.D8msr4.Hfrsr4	-	-
97	147			Apbsr4.D8msr4.Erssr4==Awdsr4.D8msr4.Erssr4	-	-
98	148			Apbsr4.D8msr4.Sbrsr4==Awdsr4.D8msr4.Sbrsr4	-	-
99	149			Apbsr4.D8msr4.Osrsr4==Awdsr4.D8msr4.Osrsr4	-	-
100	150			Apbsr4.D8msr4.Wqrsr4==Awdsr4.D8msr4.Wqrsr4	-	-

Report and Control Register Mappings

- “report_seq_mappings” provide information on
 - All the mapping points
 - All the points not mapped
- Internal mappings have significant impact on the convergence

```
vcf> report_seq_mappings -backend
-----
Initial register mappings found based on name matching.
- Note these are hints and not assumed to hold.
-----
[Mapped]          - impl.go1(1) == spec.go1(1)
[Mapped]          - impl.go2(1) == spec.go2(1)
[Mapped]          - impl.go3(1) == spec.go3(1)
[Mapped]          - impl.go4(1) == spec.go4(1)
[Mapped]          - impl.product(16) == spec.product(16)
[Mapped]          - impl.stage1(16) == spec.stage1(16)
[Mapped]          - impl.stage2(32) == spec.stage2(32)
[Mapped]          - impl.stage3(32) == spec.stage3(32)
[Mapped]          - impl.stage4(24) == spec.stage4(24)
[Mapped]          - impl.valid(1) == spec.valid(1)
[Not Mapped] - Not Found - impl.cg2.en_out(1)
[Not Mapped] - Not Found - impl.cg3.en_out(1)
[Not Mapped] - Not Found - impl.cg4.en_out(1)
-----
Total (Mapped 10) (Not mapped 3)
1
```

Results



The screenshot shows the VCF-ProofTree interface. The 'Verification Targets' table lists four items, all with a yellow warning icon and a status of 'inconclusive'. The 'Constraints' table lists three constraints: 'pl_MEMCGBYP', 'mpl_RAMHOLD', and 'K_enable_intel'. The 'Properties' section shows '547 - passed(543) - failed(4) - disabled(0)'. The 'Constraints Enabled' section shows '534'. The 'Min depth' is 4, 'Max depth' is 4, and 'Run Time' is 48:01:04.

Name	Progress	Result
seqdef	100%	#A:613:00:0:0:#C:6
rw1_1	100%	#A:613:00:0:0:#C:6
ur_1	100%	#A:613:00:0:0:#C:6
ldcp_1	100%	#A:613:00:0:0:#C:6

status (v)	depth	name
inconclusive	4	user_g_cas3_cpu01_u_cas3_cpu_u_cas3_noram_u_datarom_rdata1_1_h
inconclusive	4	user_g_cas3_cpu01_u_cas3_cpu_u_cas3_noram_u_datarom_rdata1_1_h
inconclusive	4	user_g_cas3_cpu01_u_cas3_cpu_u_cas3_noram_u_datarom_rdata1_1_h
inconclusive	4	user_g_cas3_cpu01_u_cas3_cpu_u_cas3_noram_u_datarom_rdata1_1_h

name	security	witness	usage	type	class
pl_MEMCGBYP			assume	assume	script
mpl_RAMHOLD			assume	assume	script
K_enable_intel			assume	assume	script

Properties: 547 - passed(543) - failed(4) - disabled(0) | Constraints Enabled: 534 | Min depth: 4 | Max depth: 4 | Run Time: 48:01:04

4 inconclusive after 3 days



partial word mapping
seqmap internal mapping



The screenshot shows the VCF-ProofTree interface. The 'Verification Targets' table lists four items, all with a green progress bar and a status of 'proved'. The 'Constraints' table lists three constraints: 'pl_MEMCGBYP', 'mpl_RAMHOLD', and 'K_enable_intel'. The 'Properties' section shows '547 - passed(543) - failed(0) - disabled(0)'. The 'Constraints Enabled' section shows '534'. The 'Min depth' is 4, 'Max depth' is 4, and 'Run Time' is 2:01:04.

Name	Progress	Result
seqdef	100%	#A:613:00:0:0:#C:6
rw1_1	100%	#A:613:00:0:0:#C:6
ur_1	100%	#A:670:00:2:0:0:#C:6
ldcp_1	100%	#A:57:00:0:0:0:#C:6

status (v)	depth	name
proved	4	user_g_cas3_cpu01_u_cas3_cpu_u_cas3_noram_u_datarom_rdata1_1_h
proved	4	user_g_cas3_cpu01_u_cas3_cpu_u_cas3_noram_u_datarom_rdata1_1_h
proved	4	user_g_cas3_cpu01_u_cas3_cpu_u_cas3_noram_u_datarom_rdata1_1_h
proved	4	user_g_cas3_cpu01_u_cas3_cpu_u_cas3_noram_u_datarom_rdata1_1_h

name	security	witness	usage	type	class
pl_MEMCGBYP			assume	assume	script
mpl_RAMHOLD			assume	assume	script
K_enable_intel			assume	assume	script

Properties: 547 - passed(543) - failed(0) - disabled(0) | Constraints Enabled: 534 | Min depth: 4 | Max depth: 4 | Run Time: 2:01:04

Full proof within 2 hours