Improvement of Chip Verification Automation Technology

Ma Yao, Shao Haibo, Yue Yaping, Cao Zhu

Key words: Chip verification, HVP, visualization report

Background introduction

With the continuous expansion of the scale of integrated circuits, chip verification has become more and more important in the chip development process. At the same time, chip verification has gradually developed a very complete process: from the definition of the hardware system to the post-silicon Test part. However, most companies currently have numbers of problems with the verification report generation process.

Visual verification report

In each stage of chip verification, it is neccessary to understand the verification status of each level, the individual verification progress and defect repair progress. The invention automatically generates reports that are beneficial to project management through customized configuration files, reasonably optimizes and allocates resources, and makes the project progress smoothly.A visual verification report can be generated based on the configuration file. In each stage of chip verification, verification engineers need to understand the verification status of each module, subsystem, and system, the pass rate of testcase, and the progress of each person. The configuration file and parameter description of the test report are shown in Figure 4.

```
rl_path: D:/regression/logtree  ##Regression test results storage path
report_path: D:/regression/logtree/regression_table  ##Generate report storage path
rtl_version: RTL0.8  ##RTL version
module:   ##Level of report generation: module level
  - total: 1  ##1 indicates that the total progress report is generated, sorted by date and
priority
  - spilt: 1
  - personal: all
ss:          ##Level of report generation: Subsystem level
  - total: 1
  - spilt: 1  ##1 represents the generation of progress reports for each module/subsystem,
classified according to date and module name/subsystem name
  - personal: all
soc:         ##Level of report generation: system level
  - total: 1
  - spilt: 1
  - personal: all  ##1 means to generate a personal progress report, all means to generate
a progress report for all
```

Figure4 Configuration file and parameter description of test report

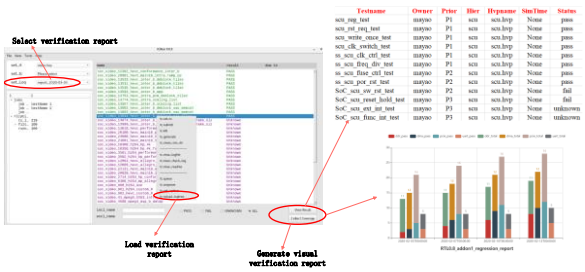

Figure5 Visual verification report integrated rendering

After the configuration file completed, the verifier only needs to get the regression test report, automatically process the regression test report, extract the testcase status and hierarchical structure related information through the script. And then it is convenient to generate the required test in the regression test tool with one click report. In a large-scale chip verification project, there may be dozens or even hundreds of subsystems and modules. In order to efficiently complete the above work, a visual and intuitive report generation method is extremely important. Through the automatic, visual, interactive, and configurable regression test report generation method, the verification manager can save a lot of time and deploy reasonably resources according to the report as shown in Figure5.

Conclusion

The automatic verification plan and visual report generation can save the verifier's time and project management tools. Related costs, while making the project schedule management and personnel deployment more reasonable.

Innovation for verification plans

This article has made two innovations for traditional project management software: 1.Innovations for verification plans; 2.Visual verification report generation.

Use HVP standard grammar rules to generate verification plans, and complete testcases through the control of attributes in HVP and the definition of hierarchical structure to complete the division of verification levels (module level, subsystem level, system level). The specific method is to use the structured verification plan (HVP) proposed by Synopsys Company to define the attributes and declarations suitable for chip verification. For the current subsystem-level report generation and extraction process commonly used by chip verification companies, as shown in Figure1.

There are three steps to generate a hierarchical structured. (1)defining attributes of hvp, the relevant functions, responsible person, and update history of each test case;(2)Complete the mapping of testcase, function coverage and verification plan through the hierarchical definition of HVP, as shown in Figure2.The definition of HVP on the left, the hierarchical structure on the right;(3)The division of modules, subsystems, and systems could be completed through the naming rules and structure definitions of testcaseas shown in Figure3.Tools can invert hvp to verification plan, as shown in Figure4.

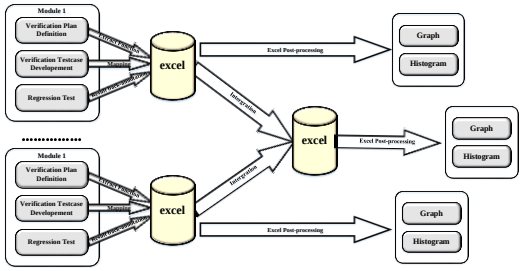

Figure1 Subsystem Level Report Generation Process

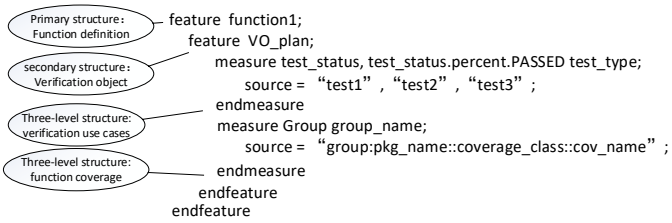

Figure2 HVP Feature Structure

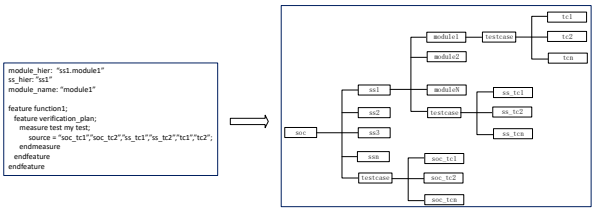

Figure3 HVP Hierarchical Definition Structure

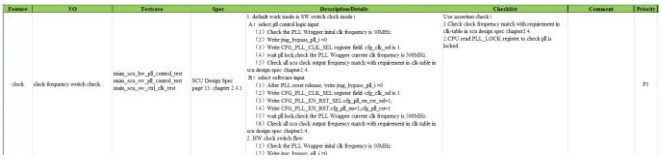

Figure4 Verification plan example